

VertiGaN: Numerical Study and Reanalysis of a Vertical GaN Transistor Concept

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VertiGaN: Numerical Study and Reanalysis of a Vertical GaN Transistor Concept

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Original numerical study at GeePs, 2022
CNRS UMR 8507 · CentraleSupélec · Gif-sur-Yvette, France

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Original study date

Revised edition, 2026

Abstract

VertiGaN is a concept for a vertical GaN transistor with two mirrored conduction cells, p-GaN gate regions and central isolation. This report reassesses the geometry and electrical plots from the 2022 Ecorce study and adds an independent calculation for a one-dimensional GaN drift layer. The archived transfer current remains of order 10^{-10} A/cm after unit conversion. The output trace reaches approximately 45.4 A/cm at 2 kV, corresponding to an apparent voltage-to-current ratio of 44 Ω·cm. Near 30 V the digitised trace gives about 2 A/cm, corresponding to about 15 Ω·cm (9–33 Ω·cm across the selected pixels). The exported Combi quantity requires a separate definition. Matching biases and terminal-current conventions across the sweeps is needed to assess gate control. The off-state export shows no resolved avalanche transition through 5 kV. For an assumed 20 µm uniform drift layer and donor density of 10^{16} cm^{-3}, two published ionisation laws predict 1.96–2.46 kV. The comparison identifies the drift profile, field convergence and avalanche settings as priorities for a device-level calculation. The available exports leave the threshold, on-resistance and breakdown voltage of the proposed device undetermined.

Keywords · gallium nitride, vertical transistor, two-dimensional electron gas, TCAD, impact ionisation, numerical verification.

Scope and data sources

The 2022 internship report [18] preserves Ecorce model views and plotted results. Appendix C reproduces the archived figures. The digitised plots use selected trace pixels to audit the displayed scales. Appendix B describes the independent electrostatic and avalanche model.

Acknowledgements

The author thanks Tanguy Phulpin for proposing the original device hypothesis and supervising the numerical work carried out at GeePs in 2022. Alain Michez provided guidance on the Ecorce semiconductor simulator and discussions on the construction and interpretation of the models. The author also acknowledges the scientific and technical staff of GeePs and CentraleSupélec.

Nomenclature

Symbol	Definition	Symbol	Definition
q, k_B	Elementary charge and Boltzmann constant	A_{active}	Active area used to normalise a device resistance
E_c, E_v, E_g	Band-edge energies and semiconductor band gap	V_{GS}, V_{DS}	Gate-to-source and drain-to-source voltages
E, E_{crit}	Electric field and critical field in an avalanche or screening model	V_{TH}, V_{BR}	Threshold voltage and breakdown voltage at stated criteria
ϕ, ε_s, ε_r	Potential, semiconductor permittivity and relative permittivity	g_m	Differential transconductance at fixed drain bias
ρ, ρ_{el}, ρ_c	Volumetric charge density, bulk electrical resistivity and specific contact resistivity	R_{on}, $R_{\text{on,sp}}$	Device on-resistance and area-normalised specific on-resistance
n, p, n_s	Electron and hole concentrations and electron sheet density	η_{sym}	Fractional imbalance of the two cell currents
N_D, N_A	Net ionised donor and acceptor concentrations	α, β	Electron and hole impact-ionisation coefficients in Appendix B
μ_n, μ_p	Electron and hole mobilities	k, L, w	Longitudinal field slope magnitude, drift-layer thickness and depleted length in Appendix B
$\mathbf{J}_n$, $\mathbf{J}_p$	Electron and hole volume current densities	V_{FD}, V_A	Full-depletion voltage and first avalanche root in Appendix B
I_D, I'_D	Drain current and drain current per unit out-of-plane depth	2DEG, HEMT	Two-dimensional electron gas and high-electron-mobility transistor
I'_{crit}, I'_{floor}	Specified current-per-depth criterion and numerical current floor	Ecorce, TCAD, FEM	Device simulator, technology computer-aided design and finite-element method
W, p_{pitch}	Out-of-plane extrusion depth and in-plane active pitch		

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1 Research Context and Numerical Methodology

1.1 Research question and scope

The original device calculations were performed at the GeePs laboratory, CNRS UMR 8507, CentraleSupélec, in 2022. They examined a vertical GaN transistor architecture intended for enhancement-mode operation, represented the geometry in Ecorce and compared its electrical signatures with three reference device families. This reanalysis examines the recorded geometry, physical assumptions and electrical exports and adds a reduced-model test of the drift layer.

A numerical device model predicts responses conditional on its geometry, physical models and numerical settings. The simulation can be represented as follows.

$$M(\theta, \mathbf{b}, P, N) \longrightarrow \mathbf{y} \tag{1.1}$$

Here M is the device model, θ contains the geometric and material parameters, $\mathbf{b}$ is the applied bias vector, P denotes the selected physical models, N denotes the discretisation and solver tolerances, and $\mathbf{y}$ is the predicted response.

The analysis addresses three questions.

1. Can the proposed architecture create a gate-controlled conduction path while preserving a vertical blocking region?
2. Do the exported curves describe a consistent device under a common geometry, material model, unit convention and bias sequence?
3. Which metrics can be extracted from the available exports, and which require new calculations or measurements?

Research contribution

The archived Ecorce model represents the proposed architecture, while the recorded bias conditions, unit conventions and solver diagnostics leave several questions open. These gaps identify the calculations needed to assess the device.

1.2 Numerical workflow

The workflow used the Ecorce simulator [13] to specify device geometry, materials, contacts, transport equations and terminal bias. Current, charge, potential and post-processing quantities were exported for analysis. The original device input files and raw per-terminal currents were not available for this reanalysis.

The calculation and its diagnostics form an iterative workflow.

$$\begin{aligned}&\text{Hypothesis} \rightarrow \text{Geometry} \rightarrow \text{Models} \rightarrow \text{Mesh}\\ &\rightarrow \text{Bias sweep} \rightarrow \text{Diagnostics} \rightarrow \text{Revision}\end{aligned} \tag{1.2}$$

A small residual establishes convergence for the discretised equations. Charge and current conservation, mesh refinement and physical calibration are needed to assess the resulting device predictions [9].

1.3 Governing equations

1.3.1 Electrostatics and carrier transport

The continuum formulation couples electrostatics, transport and continuity [6, 9]. The electrostatic potential ϕ obeys Poisson's equation.

$$\begin{aligned}\nabla \cdot (\varepsilon_s \nabla \phi) = -q\,(p - n + N_D^+ - N_A^-)\\ -\rho_{\text{fix}} - \rho_{\text{trap}}\end{aligned} \tag{1.3}$$

Here ρ_{fix} and ρ_{trap} are fixed and trapped volumetric charge densities. Sheet charges at abrupt interfaces enter through the corresponding electrostatic boundary conditions.

In a drift–diffusion formulation, the electron and hole current densities are

$$\mathbf{J}_n = q\mu_n n\mathbf{E} + qD_n \nabla n \tag{1.4}$$

$$\mathbf{J}_p = q\mu_p p\mathbf{E} - qD_p \nabla p \tag{1.5}$$

With $\mathbf{E} = -\nabla\phi$, the steady-state continuity equations are

$$\nabla \cdot \mathbf{J}_n = q(R - G) \tag{1.6}$$

$$\nabla \cdot \mathbf{J}_p = q(G - R) \tag{1.7}$$

Here R and G are recombination and generation rates. Mobility, recombination, incomplete ionisation and high-field transport models determine the range of validity of the drift–diffusion solution [6, 10].

1.3.2 Quantum confinement as a modelling option

Carriers at AlGaN/GaN interfaces can occupy confined subbands [1, 2, 10]. One modelling option is to solve the effective-mass Schrödinger equation along the confinement direction and couple it to Poisson's equation.

$$\left[-\frac{\hbar^2}{2}\frac{\mathrm{d}}{\mathrm{d}z}\left(\frac{1}{m^*(z)}\frac{\mathrm{d}}{\mathrm{d}z}\right) + E_c(z)\right]\psi_i(z) = E_i\psi_i(z) \tag{1.8}$$

The occupied subbands supply the charge density used in equation (1.3). A self-consistent calculation iterates until a stated tolerance is met.

$$\left\|\phi^{(k+1)} - \phi^{(k)}\right\|_\infty < \varepsilon_{\text{PS}} \tag{1.9}$$

The Schrödinger–Poisson formulation is included as background for the interface physics. The archived VertiGaN exports do not establish that a self-consistent quantum solver was used for the reported sweeps.

1.3.3 Nonlinear solution and convergence diagnostics

For a discretised nonlinear system $\mathbf{F}(\mathbf{u}) = \mathbf{0}$, Newton's method updates the state vector according to

$$\begin{aligned}\mathbf{J}_F(\mathbf{u}^{(k)})\,\Delta\mathbf{u}^{(k)} &= -\mathbf{F}(\mathbf{u}^{(k)})\\ \mathbf{u}^{(k+1)} &= \mathbf{u}^{(k)} + \alpha_k \Delta\mathbf{u}^{(k)}\end{aligned} \tag{1.10}$$

The damping factor α_k controls each Newton step. Residuals, terminal-current imbalance, iteration count and maximum field should be recorded for every bias point [9]. These diagnostics were not systematically retained with the 2022 exports.

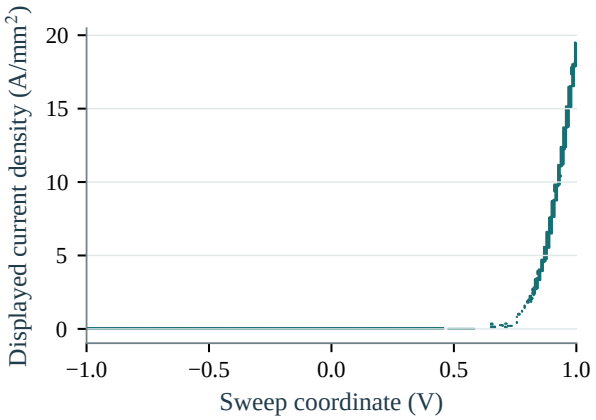

Figure 1.1 – Silicon diode trace digitised from the 2022 Ecorce export. The original ordinate is current density in A/mm^2. The trace illustrates rectification for the archived model.

1.4 Initial simulator verification

An archived silicon diode calculation (Figure 1.1) exhibits rectification under the applied voltage ramp. The original Ecorce plot appears in Figure C.1a. The magnitude depends on its device and boundary settings. Analytical depletion width, built-in voltage, low-injection current and terminal-current conservation provide quantitative checks [6, 9].

1.5 Dimensional normalisation in two-dimensional TCAD

In an extruded two-dimensional device, I'_D is the drain current per unit out-of-plane depth. The drain current I_D is obtained for an extrusion depth W expressed in the same length unit.

$$I_D = I'_D W \tag{1.11}$$

Specific on-resistance is obtained from the device resistance using the active area.

$$R_{\mathrm{on,sp}} = R_{\mathrm{on}} A_{\mathrm{active}} \tag{1.12}$$

For a structure of in-plane active pitch p_{pitch} and extrusion depth W, $A_{\mathrm{active}} = p_{\mathrm{pitch}} W$. The product $(V_{\mathrm{DS}}/I'_D) \times p_{\mathrm{pitch}}$ then has units of $\Omega{\cdot}\mathrm{cm}^2$ when the length convention is centimetres. Comparisons across devices require matched area, cell count, contact treatment and bias.

2 Device-Physics Basis for a Vertical Normally-Off GaN Transistor

2.1 The power-switch design space

The choice of a power switch depends on voltage rating, conduction loss, switching energy, gate drive and temperature [3, 7, 12]. For a unipolar switch the first-order conduction loss is

$$P_{\mathrm{cond}} \simeq I_{\mathrm{rms}}^2 R_{\mathrm{on}} \tag{2.1}$$

and a first-order switching and gate-drive loss budget at frequency f_s can be written as

$$P_{\mathrm{sw}} \simeq \frac{1}{2} V_{\mathrm{DS}} I_D (t_r + t_f) f_s + Q_G V_{\mathrm{drv}} f_s + E_{\mathrm{oss}} f_s \tag{2.2}$$

The terms represent voltage–current overlap, gate-drive energy and the dissipated contribution of the output capacitance. The last contribution depends on the commutation circuit. Resistance, charge and the operating voltage must therefore be considered together [7, 12].

The comparison of power-device families motivates the use of majority-carrier wide-band-gap devices. For this architecture, the design problem is the distribution of electric field, charge and heat while maintaining gate control and a feasible fabrication route.

2.2 Why gallium nitride is attractive

GaN has a wide band gap, a large critical electric field and a polar wurtzite crystal structure [3, 5, 10, 17]. Reported lateral and vertical devices illustrate the trade-offs between gate structure, voltage support and manufacturability [4, 11].

For an ideal unipolar drift region, one-dimensional Baliga scaling gives the following dependence on breakdown voltage and semiconductor parameters [7].

$$R_{\mathrm{on,sp}}^{\mathrm{ideal}} \propto \frac{V_{\mathrm{BR}}^2}{\varepsilon_s \mu_n E_{\mathrm{crit}}^3} \tag{2.3}$$

The cubic dependence on E_{crit} explains the voltage scaling advantage of wide-band-gap materials in the ideal model. Channel, access and contact resistance, field crowding and thermal effects change the device result. Figure 2.1 gives a material comparison and a dimensionless illustration of the scaling.

2.3 Formation of the AlGaN/GaN two-dimensional electron gas

In AlGaN/GaN HEMTs, discontinuities in spontaneous and piezoelectric polarisation produce sheet charge and alter the conduction-band profile. Electrons can occupy a quantum well near the heterointerface and form a two-dimensional electron gas (2DEG) [1, 2, 10]. Figures 2.2 and 2.3 illustrate the layer sequence and band-edge change.

The following simplified electrostatic relation illustrates the dependence of the sheet density on polarisation, barrier thickness and band alignment [2].

$$n_s(x) = \frac{\sigma_{\mathrm{pol}}(x)}{q} - \frac{\varepsilon_0 \varepsilon_{\mathrm{AlGaN}}(x)}{q^2 d_b} \times \left[q\phi_B + E_F(n_s) - \Delta E_c(x) \right] \tag{2.4}$$

Here d_b is the barrier thickness, σ_{pol} is the net polarisation sheet charge, ϕ_B is the Schottky barrier potential and ΔE_c is the conduction-band offset. The barrier composition and thickness affect both polarisation and the gate electrostatics.

Table 2.1 – Physical comparison of representative power-transistor families.

Family	Control	Dominant strength	Principal limitation
BJT	Base current	Low conduction drop at moderate voltage	Minority-carrier storage and continuous drive current
MOSFET	Insulated gate	Fast majority-carrier switching and simple drive	Drift resistance rises with blocking voltage in silicon
IGBT	Insulated gate with bipolar conduction	High current and voltage capability	Tail current limits high-frequency switching
Lateral GaN HEMT	Field-controlled 2DEG	High mobility, low charge and high-frequency operation	Lateral field crowding, surface trapping and voltage–area trade-off
Vertical wide-band-gap FET	Field-controlled vertical path	Voltage scaling through drift thickness and compact area	Epitaxy, defect control, contact technology and gate reliability

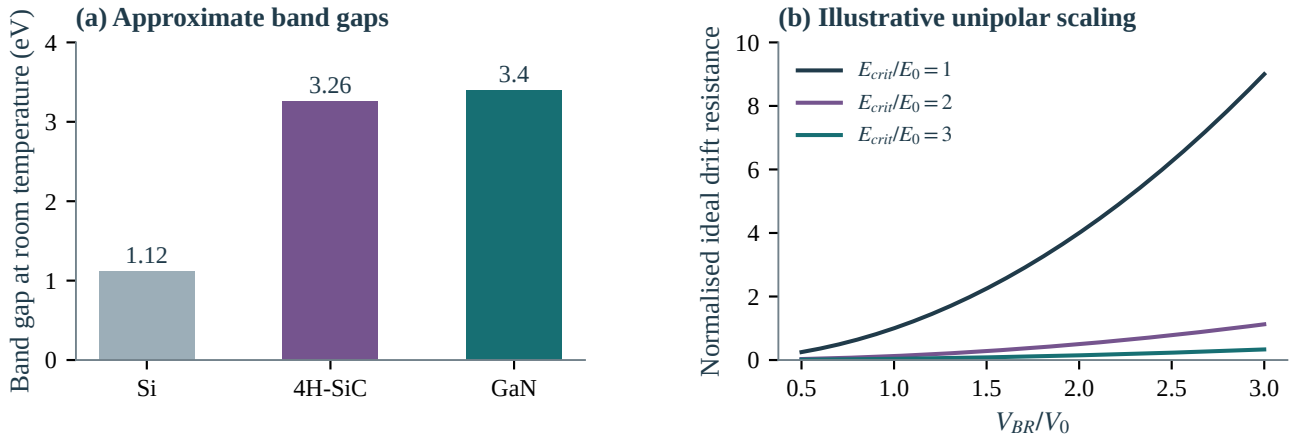

Figure 2.1 – Drawn for this report using approximate room-temperature band gaps from [17] and the scaling in equation (2.3). Panel (b) varies the critical field at fixed mobility and permittivity. Its axes are dimensionless.

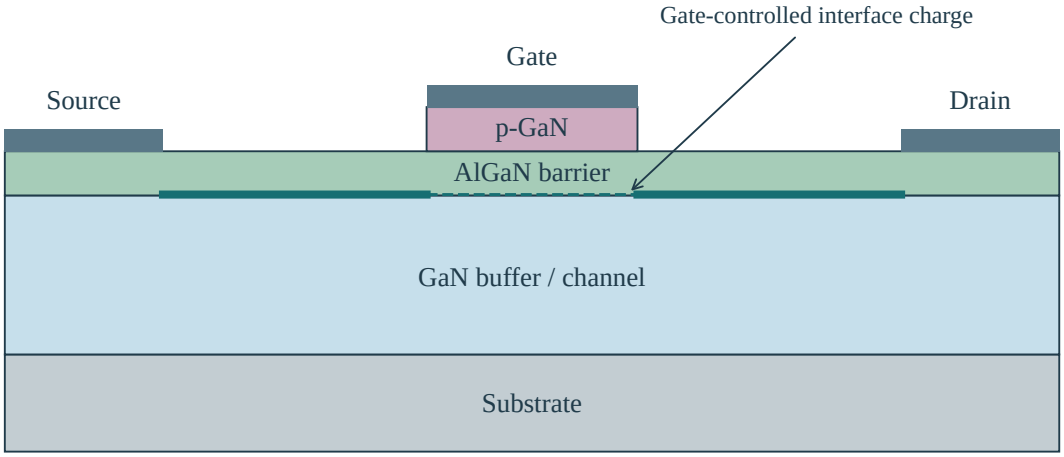

Figure 2.2 – Drawn for this report. Generic lateral p-GaN gate HEMT showing the heterointerface and gate-controlled region [1, 2, 5]. Layer heights are schematic.

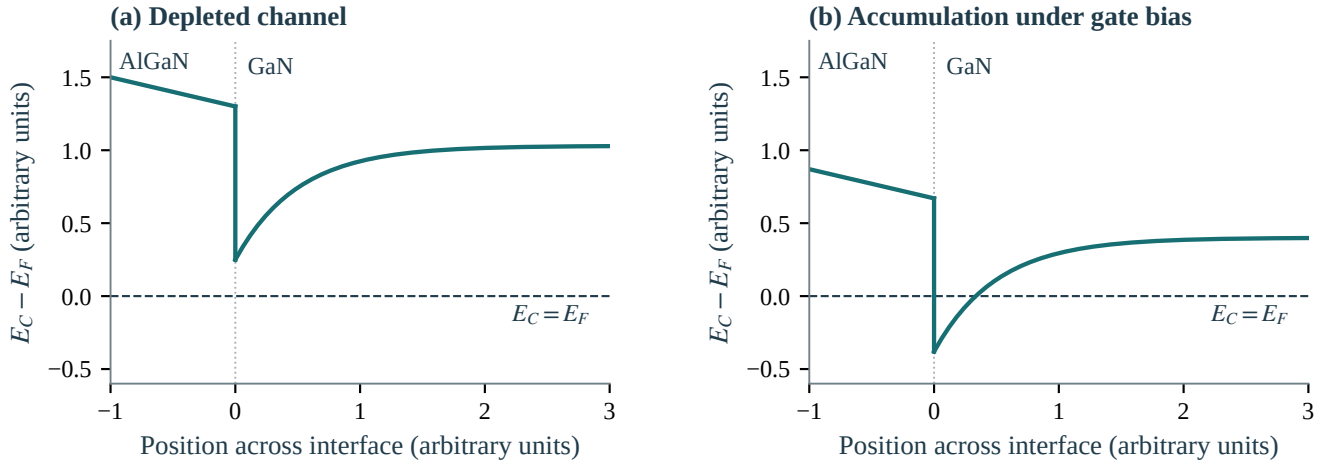

Figure 2.3 – Drawn for this report. Schematic conduction-band profiles for depleted and accumulated channel conditions, with an illustrative slope in the AlGaN barrier. Horizontal and vertical scales use arbitrary units [1, 2].

2.4 Enhancement-mode operation

AlGaN/GaN heterostructures can support a channel near zero gate bias. Recessed gates, gate dielectrics, ion treatment and p-GaN gate layers are among the approaches to a positive threshold. Cascode configurations obtain external normally-off operation through circuit topology [3–5, 11, 12]. VertiGaN uses a p-GaN gate region as a design hypothesis.

Ionised acceptors and band bending in a p-GaN gate region can deplete the channel beneath the gate [5, 10]. A sheet-charge perturbation Q_s shifts the threshold through the effective gate capacitance per unit area C_g.

$$\Delta V_{\mathrm{TH}} \simeq -\frac{Q_s}{C_g} \tag{2.5}$$

The charge budget sets one contribution to the threshold. Interface charge and traps can also shift V_{TH} with bias history. Figure 2.4 illustrates transfer curves with negative and positive threshold voltages.

The differential transconductance uses a fixed drain bias. A threshold extraction additionally specifies a current-per-depth criterion I'_{crit}, temperature, sweep direction and the treatment of gate leakage [5, 8].

$$g_m(V_{\mathrm{GS}}) = \left.\frac{\partial I_D}{\partial V_{\mathrm{GS}}}\right|_{V_{\mathrm{DS}}} \tag{2.6}$$

$$I'_D(V_{\mathrm{TH}}, V_{\mathrm{DS}}; T) = I'_{\mathrm{crit}} \tag{2.7}$$

Linear extrapolation in a specified region provides an alternative threshold convention. A wide-interval secant slope describes an average response.

2.5 Traps, dynamic resistance, and reliability

Traps at surfaces, in the buffer and at dielectric interfaces may capture and emit carriers [5, 8, 10]. A first-order occupancy model for a single electron trap has the following form.

$$\frac{\mathrm{d}f_t}{\mathrm{d}t} = c_n n(1 - f_t) - e_n f_t \tag{2.8}$$

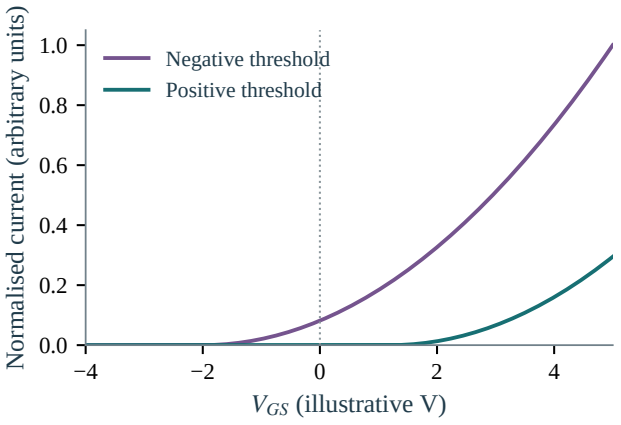

Figure 2.4 – Drawn for this report. The negative- and positive-threshold curves use a squared positive gate overdrive. Current is shown in arbitrary units. Threshold extraction requires a stated current criterion, drain bias, temperature, sweep direction and gate-leakage check.

where c_n and e_n are capture and emission coefficients. The emission time constant often follows an Arrhenius dependence,

$$\tau_e^{-1} \propto \sigma_n v_{\mathrm{th}} N_C \exp\left(-\frac{E_C - E_T}{k_B T}\right) \tag{2.9}$$

The activation energy can be estimated from emission-rate measurements over a stated temperature and bias range [8]. The archived VertiGaN curves contain no temperature-dependent trap data.

Trapped charge can reduce channel charge after off-state stress and increase dynamic on-resistance [5, 12]. Pulsed I–V, gate leakage and recovery measurements are needed to assess these effects.

2.6 Why a vertical architecture changes the design problem

In a lateral HEMT, the gate–drain spacing simultaneously sets the blocking length, surface-field profile, device area,

and access resistance. In a vertical architecture, the blocking voltage can be supported by a drift region approximately normal to the wafer surface. For an ideal uniformly doped one-sided region,

$$W_D \simeq \sqrt{\frac{2\varepsilon_s V_{\mathrm{BR}}}{qN_D}} \tag{2.10}$$

$$E_{\max} \simeq qN_D W_D/\varepsilon_s \tag{2.11}$$

This separates voltage scaling from lateral footprint, but it introduces demanding requirements on epitaxial thickness, defect density, edge termination, vertical contacts, substrate conduction, and heat removal.

The VertiGaN proposal should therefore be understood as a field-management hypothesis: it attempts to preserve a gate-controlled GaN channel while redirecting the main current and blocking-field path vertically. The concept is examined in the next chapter.

3 VertiGaN Architecture and Simulation Protocol

3.1 Architectural hypothesis

VertiGaN consists of two mirrored conduction cells separated by a central region. Each has a source, a drain and a p-GaN region adjacent to the gate. Six terminals allow evaluation of independent and parallel bias conditions. The axial conduction paths and the gate-charge control mechanism are the design features under study (Figure 3.1).

Four hypotheses guide the device analysis.

1. p-GaN or an equivalent fixed-charge region depletes each gate-controlled channel at zero bias;
2. positive gate bias restores a conductive channel with acceptable transconductance;
3. the vertical drift path supports a larger voltage than a comparable lateral gate–drain access region;
4. parallel operation increases the current carried by the footprint while keeping gate-edge and dielectric fields within the selected design limits.

The hypotheses interact. Stronger p-type depletion can raise the threshold and channel resistance. A thicker dielectric can alter leakage and local field concentration. Parallel cells may increase total current while introducing thermal imbalance.

3.2 Two-dimensional implementation

The archived Ecorce cross-section indicates a nominal height of 20 µm and pitch of 10 µm. Each GaN region is about 3 µm wide. The centre comprises an approximately 0.8 µm SiO_2 strip flanked by two Si regions of about 0.6 µm each (Figure 3.2 and Figure C.7b). The Si doping, electrical contacts and interface conditions were not recorded with the export. These regions can affect voltage partition across the cell. The geometry does not supply a drift-layer donor density.

At a common extrusion depth, the currents of two parallel cells add according to their signed terminal definitions.

$$I_{D,\mathrm{tot}} = I_{D,1} + I_{D,2} \tag{3.1}$$

provided both branches use the same sign convention and no terminal is inadvertently floating. Symmetry can be checked through

$$\eta_{\mathrm{sym}} = \frac{|I'_{D,1} - I'_{D,2}|}{|I'_{D,1}| + |I'_{D,2}|} \tag{3.2}$$

which should be close to zero when the two cells have equivalent geometry, material orientation, polarisation charges, contacts and bias. This diagnostic was not exported in the original study and should be added in future runs.

3.3 Contacts and material interfaces

Metallic atomic density and semiconductor interface charge are distinct physical quantities. Contact models should specify the work function and boundary condition, while interface and transport models require the following inputs [6, 8].

- metal work function and Schottky-barrier height;
- specific contact resistivity ρ_c and transfer length;
- fixed interface charge Q_f and interface-trap density D_{it};
- bulk conductivity and geometric series resistance.

For a uniform conductor, the elementary resistance relation remains

$$R = \rho_{\mathrm{el}} L/A \tag{3.3}$$

Here ρ_{el} is the bulk electrical resistivity, L the conduction length and A the conducting cross-section. For an ohmic semiconductor contact, the specific contact resistivity ρ_c is expressed in $\Omega{\cdot}\mathrm{cm}^2$. Transmission-line measurements can help separate contact and access resistance [8].

For a solid SiO_2 region, a field-times-thickness estimate is a first screen for dielectric stress.

$$V_{\mathrm{BD,ox}} \simeq E_{\mathrm{BD,ox}} t_{\mathrm{ox}} \tag{3.4}$$

Corner fields, interface states, defects, tunnelling and time-dependent breakdown affect the allowable voltage of the processed dielectric [6, 10].

3.4 Bias experiments and extraction rules

Four numerical experiments are required to characterise each device consistently.

3.4.1 Transfer characteristic

Sweep V_{GS} at each fixed V_{DS} and temperature. Extract V_{TH}, subthreshold slope and g_m using stated conventions. Record gate leakage and both sweep directions to assess hysteresis.

3.4.2 Output characteristic

For multiple gate biases, sweep V_{DS} and separate the linear region, current-saturation region, and high-field degradation. The differential resistance near the origin is

$$R_{\mathrm{on}}(V_{\mathrm{GS}}) = \left(\frac{\partial I_D}{\partial V_{\mathrm{DS}}}\bigg|_{V_{\mathrm{DS}}\to 0^+} \right)^{-1} \tag{3.5}$$

A resistance derived from an undefined post-processing variable cannot be compared directly with this quantity.

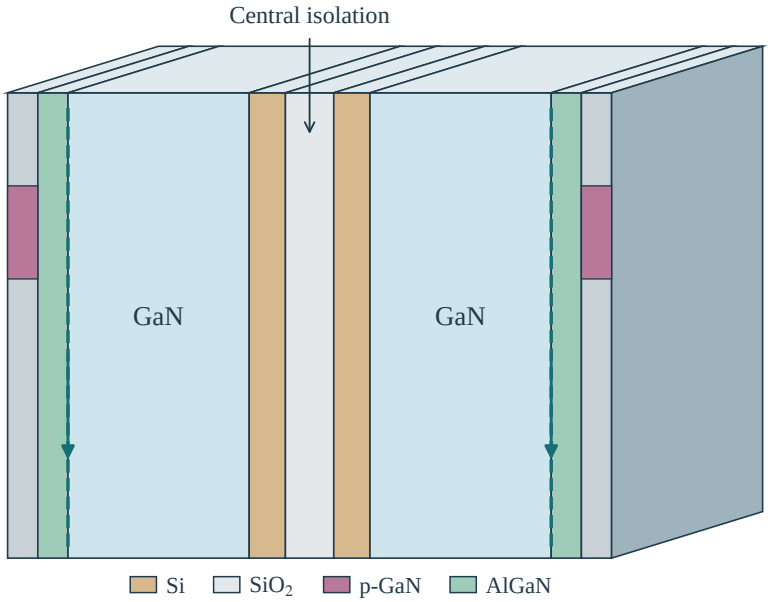

Figure 3.1 – Schematic redrawn from the 2022 concept. Two GaN conduction paths flank the central isolation region. The drawing shows the nominal topology in projection.

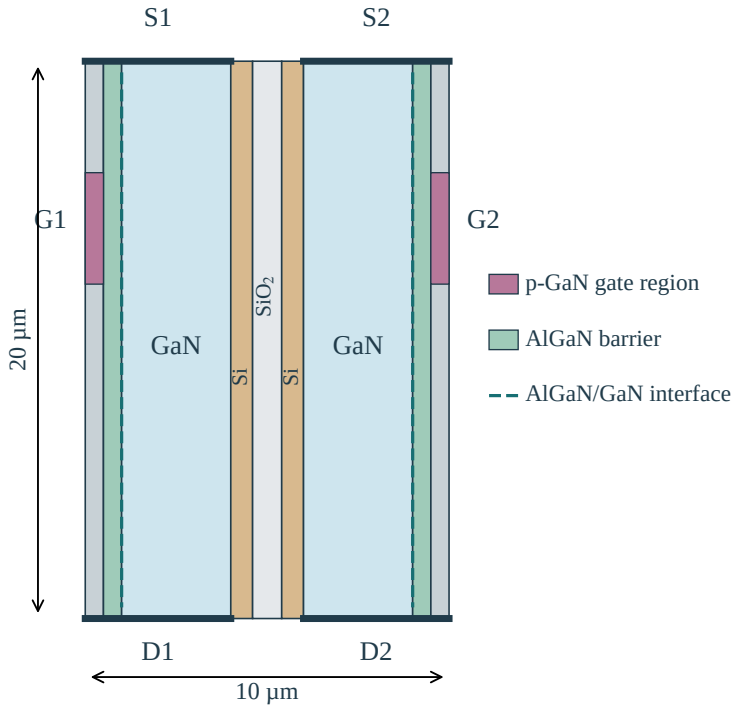

Figure 3.2 – Cross-section reconstructed from the archived Ecorce geometry, with English labels. The central SiO_2 strip is flanked by two Si strips. Contacts S1/S2, G1/G2 and D1/D2 label the source, gate and drain of each cell. Drift doping and electrical conditions in the Si strips are unavailable.

Table 3.1 – Principal VertiGaN design parameters and their first-order trade-offs.

Parameter	Intended effect	Competing risk
p-GaN acceptor density and thickness	Positive threshold and channel depletion	Mobility degradation, incomplete ionisation and high access resistance
Gate length and overlap	Improved electrostatic control	Increased gate charge and field crowding
Vertical drift thickness	Increased blocking voltage	Increased drift resistance and epitaxial cost
Drift doping	Lower resistance	Reduced depletion width and lower breakdown voltage
Central dielectric thickness	Electrical isolation between mirrored cells	Oxide field concentration and process complexity
Channel spacing	Current sharing and thermal separation	Larger cell pitch and parasitic resistance
Contact resistivity	Lower conduction loss	Process-specific metallisation and anneal
Edge termination	Reduced peak field	Added area and fabrication complexity

3.4.3 Off-state sweep

At the specified off-state V_{GS} and temperature, increase the positive drain bias. A current-based breakdown criterion uses a separately specified I'_{crit}; its numerical value can differ from the threshold criterion in equation (2.7).

$$V_{BR} = V_{DS}\big|_{I'_D = I'_{crit}} \tag{3.6}$$

A simplified high-field screening integral is

$$\int_0^L \alpha_n(E(x))\,\mathrm{d}x \simeq 1 \tag{3.7}$$

where α_n is the electron ionisation coefficient. The two-carrier feedback criterion in Appendix B is used for the separate avalanche calculation [14, 15].

3.4.4 Field and thermal maps

At every critical bias, record $|\mathbf{E}|$, current density, carrier density, potential, and lattice temperature. The local volumetric heat generation includes Joule heating,

$$q'''_J = \mathbf{J} \cdot \mathbf{E} \tag{3.8}$$

and should be coupled to the heat equation when current density is large.

3.5 Design parameters and expected sensitivities

The design objectives include threshold, on-resistance, charge, temperature and field. A weighted cost for a trial geometry can combine dimensionless ratios as follows.

$$\begin{aligned} J_{cost}(\theta) = {} & w_R \frac{R_{on,sp}}{R_0} + w_Q \frac{Q_G}{Q_0} + w_T \frac{\Delta T_{max}}{T_0} \\ & + w_E \frac{E_{max}}{E_{allow}} + w_V \max\left(0, 1 - \frac{V_{BR}}{V_{target}}\right)^2 \end{aligned} \tag{3.9}$$

The weights specify the trade-offs, and the denominators are reference values. Constraints include $V_{TH} > 0$, gate leakage, thermal limits and process feasibility.

3.6 Benchmarking strategy

The original Ecorce study includes a lateral GaN HEMT, a lateral SiC MOSFET and a vertically contacted SiC structure labelled JFET. Their transfer, output, resistance-related and off-state traces provide qualitative comparisons. Quantitative comparison requires matched biases, geometry, material models and area conventions.

3.7 Predefined falsification tests

To avoid confirmation bias, the architecture should be judged against failure conditions defined before the next simulations are run. One proposed acceptance test is a transfer-current increase of six decades above a measured numerical floor under a stated positive gate bias. Its suitability depends on the intended current range and leakage criterion. The mirrored-cell hypothesis fails if η_{sym} remains significant under nominally symmetric conditions after mesh convergence. The vertical-blocking hypothesis fails if the peak field localises at a gate or dielectric corner and reaches the calibrated critical field before the drift region is substantially depleted. Finally, the loss hypothesis fails if the sum of channel, drift, and contact resistance does not improve the relevant voltage-class benchmark after equal-area normalisation.

Each comparison should use the same extraction convention and its preselected pass criterion.

4 Benchmark Device Simulations

Appendix C reproduces the original Ecorce sweeps and cross-sections of the three benchmark structures [18].

4.1 Lateral GaN HEMT

The archived lateral GaN benchmark has an AlGaN/GaN channel, a p-GaN gate region and source and drain contacts (Figure 4.1a). The two transfer exports are treated as separate traces because their fixed drain biases, reference potentials and current definitions are unavailable.

Export A shows an apparent onset near 4.4 V in the source interpretation and reaches about 3.2 A/cm at a 15 V sweep coordinate (Figure 4.1b). Export B starts rising around −3 V, shows about 2.7 A/cm at zero on its sweep axis and reaches 19.5 A/cm near 10 V (Figure 4.2a). The Ecorce voltage axes were both labelled Pot. Under a common gate-voltage reference and matched bias the two traces would imply different turn-on behaviour. Their available metadata do not support pooling a threshold from A with a current from B.

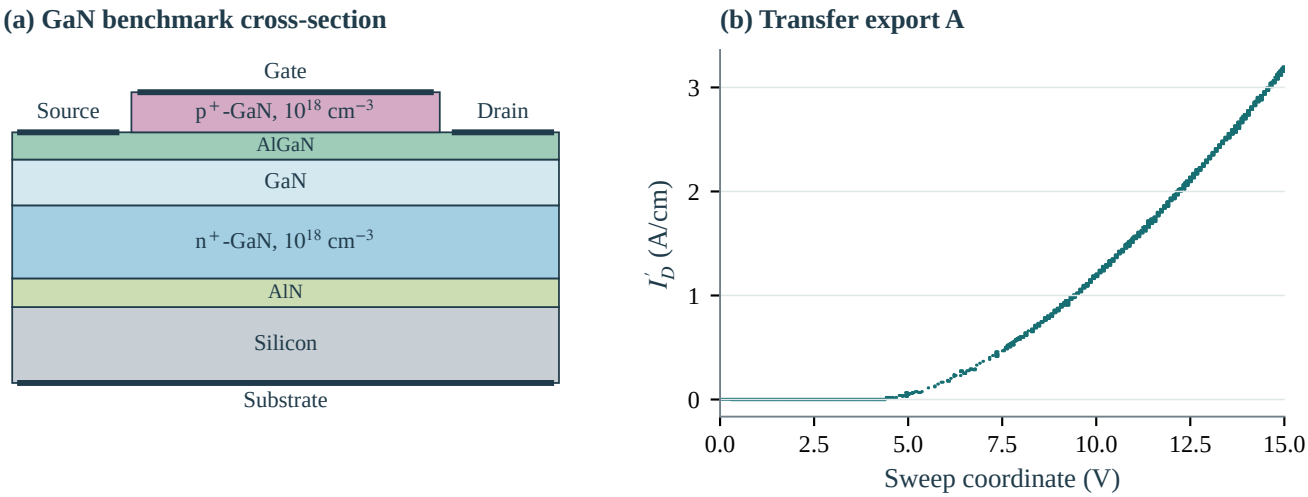

Figure 4.1 – Schematic of the archived GaN benchmark cross-section (a) and digitised transfer export A (b). Doping labels reproduce the nominal archive values. The current axis is reconstructed in A/cm.

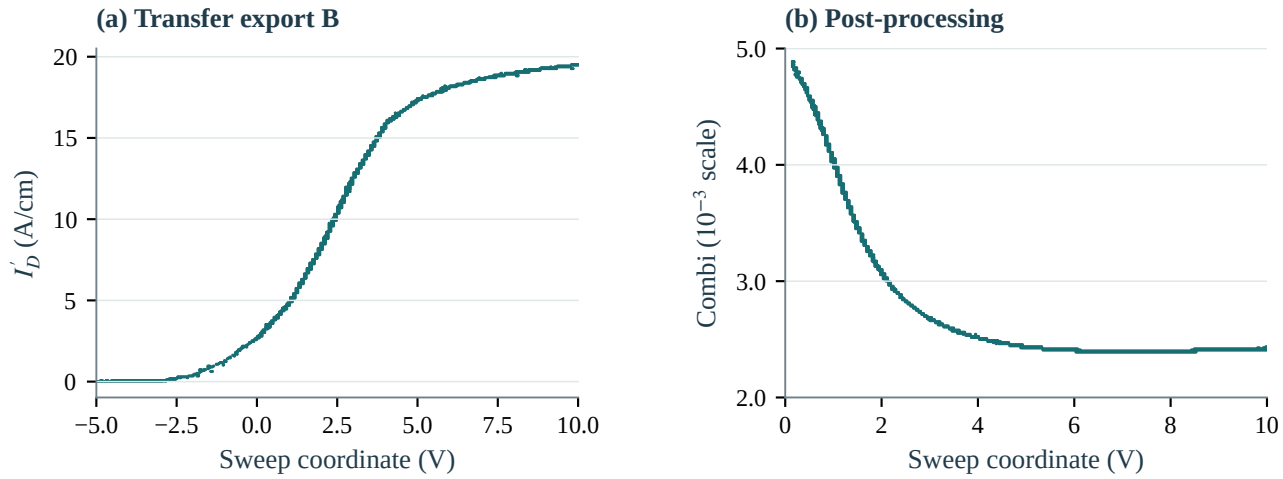

Figure 4.2 – Transfer export B (a) and its separately exported Combi trace (b). Both are digitised from the 2022 archive. The fixed bias and terminal-current definition required to match export A are unavailable.

The historical 302 mS/cm secant transconductance estimate cannot be assigned to a matched operating point. The Combi trace in Figure 4.2b levels off near 2.4×10^{-3} between 6 and 10 V on the sweep axis. Its definition and units require the archived solver configuration.

The archived HEMT cross-section (Figure 4.1a and Figure C.8a) shows an n^+-GaN layer beneath the channel region. If source and drain couple electrically to that layer, bulk conduction through it could contribute to export B. Bias-matched current-density maps and the contact definitions are needed to test this hypothesis.

4.2 Lateral SiC MOSFET

The archived lateral SiC MOSFET cross-section shows n-type source and drain regions in a p-type body on a p^+ substrate (Figures 4.3a and C.8b). No dedicated drift region is visible in the cross-section. The transfer sweep provides a comparison for gate control in a structure without a polar heterointerface.

The original interpretation gives an apparent threshold near 1 V and a secant transconductance near 142 mS/cm. The separate output trace approaches 3.27 A/cm at the end of its displayed range. Table 4.1 reports these values with their source conditions and limitations.

The original text reports 978 mΩ/cm for a resistance-related quantity. The export provides no expression that would make it comparable with a device resistance in Ω or a specific resistance in Ω·cm^2. The digitised off-state current rises towards the last plotted bias of about 620 V, which supplies no independently validated breakdown threshold.

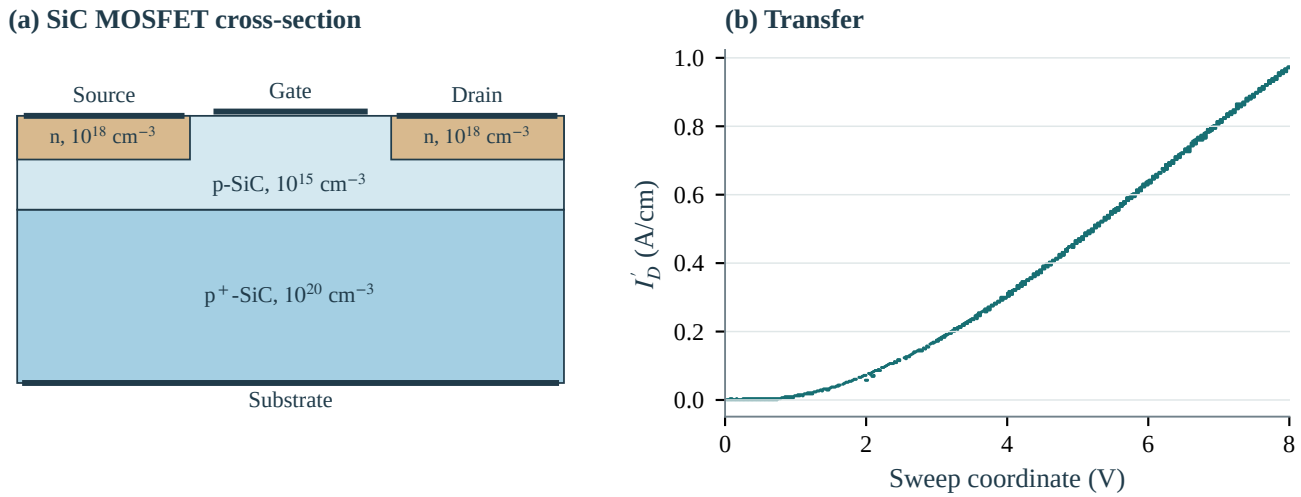

Figure 4.3 – Schematic of the archived lateral SiC MOSFET cross-section (a) and digitised transfer curve (b). Doping labels reproduce the nominal archive values.

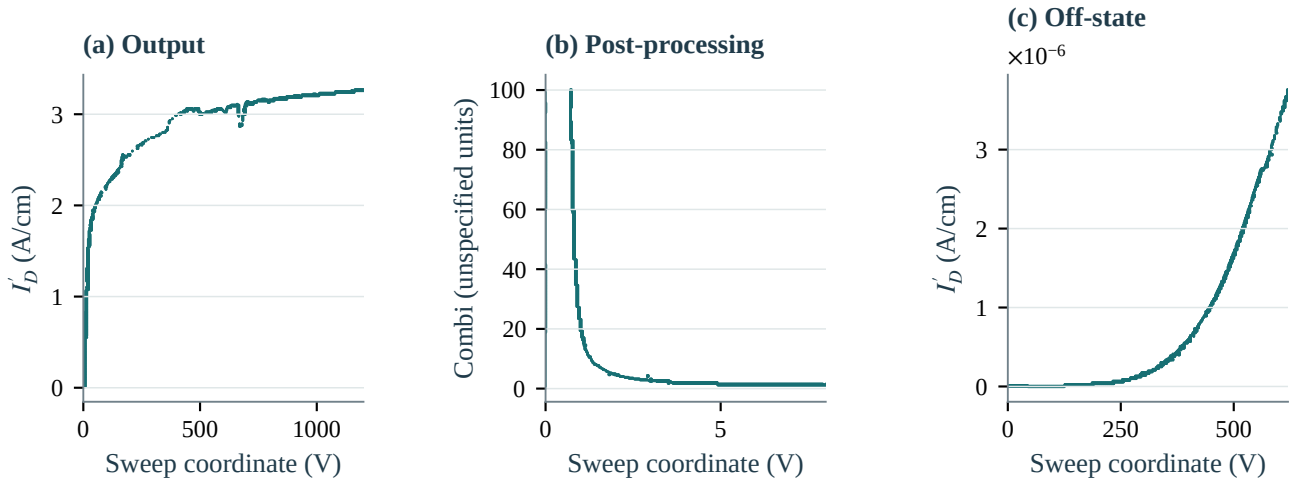

Figure 4.4 – Digitised lateral SiC MOSFET characteristics. The output and off-state currents are expressed in A/cm. Combi is shown on its native numeric axis.

4.3 Vertical SiC structure (labelled JFET)

The archived SiC structure is labelled JFET and places source and drain on opposite faces, with lateral gate contacts (Figures 4.5 and C.8c). In the archived geometry the p^+ region spans the full width, leaving no continuous n-type path between source and drain. A continuous path is necessary for conventional n-channel JFET operation.

The transfer export has an apparent onset near 2 V. The separate output export reaches about 0.299 A/cm. The original text reports a resistance near 2 Ω. The bias, geometry and extraction convention are needed to connect these quantities. The archived sweeps leave the origin of the current unresolved.

4.4 Cross-benchmark interpretation

The benchmark traces illustrate gate control and the numerical behaviour of the three geometries. Quantitative ranking requires common area conventions, bias, material models, temperature, contact treatment and extraction criteria. In particular, the lateral GaN transfers require a shared bias and gate reference before their apparent thresholds can be compared.

5 VertiGaN Numerical Results and Critical Interpretation

5.1 Transfer characteristic

The digitised transfer trace (Figure 5.1a) shows a shallow apparent onset near a 1.7 V sweep coordinate. The current is of order 10^{-14} A/µm on the original axis, or 10^{-10} A/cm after depth conversion. Numerical residuals, a gate-leakage trace and a measured solver floor are needed to interpret such small values. Appendix C.5 preserves the original axes and units (Figures C.10 and C.11).

Table 4.1 – Displayed or reported values for the benchmark structures. Each row identifies the relevant export. A threshold and an endpoint from separate traces require matched conditions.

Device or export	Apparent onset	Displayed current	Conditions and limitations
Lateral GaN, transfer A	Near 4.4 V	3.2 A/cm at 15 V	Source turn-on interpretation. Fixed drain bias and reference potential unavailable.
Lateral GaN, transfer B	Rise near −3 V	19.5 A/cm at 10 V	About 2.7 A/cm at zero on the sweep axis. Keep separate from A.
Lateral SiC MOSFET	Near 1 V	3.27 A/cm in output	p-type body on a p^+ substrate. The archive shows no dedicated drift region. Values are from separate sweeps.
Vertical SiC (labelled JFET)	Near 2 V	0.299 A/cm in output	The p^+ region spans the full width, leaving no continuous n-type path. Values are from separate sweeps.

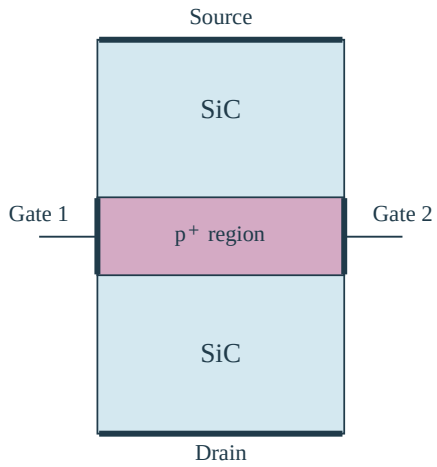

Figure 4.5 – Schematic of the archived vertical SiC structure labelled JFET. Source and drain are on opposite faces, with lateral gate contacts. Dimensions and dopant concentrations are unspecified.

Threshold extraction requires a physically stated current criterion and a resolved signal above the numerical floor I'_{floor}.

$$\frac{\left|I'_D(V_{\text{GS}} > V_{\text{TH}})\right|}{I'_{\text{floor}}} \gg 1 \tag{5.1}$$

The available transfer plot gives no validated threshold according to this criterion. Fixed drain bias, absolute gate reference and terminal-current selection remain undetermined.

5.2 Output characteristic

The digitised output trace (Figure 5.1b) reaches approximately 45.4 A/cm at a sweep coordinate near 2 kV. Interpreting the axes as drain voltage and drain current per unit depth gives $V_{\text{DS}}/I'_D \approx 44\,\Omega\cdot\text{cm}$ at that point. This is a secant ratio at a high voltage, well outside the low-voltage regime used to determine on-resistance. Near 30 V the trace gives approximately 2 A/cm, corresponding to an apparent ratio near 15 Ω·cm (9–33 Ω·cm across the selected pixels). Appendix A.3 gives the extraction resolution and historical value.

A comparison of the transfer and output traces requires a common terminal-bias vector, contact set, geometry, material model and signed-current definition. The recorded current should agree at matching states, subject to the specified sweep history and numerical tolerance. The original exports leave several possible causes for the differences.

- terminal definitions or summed current branches;
- gate bias or source reference;
- current normalisation or out-of-plane depth;
- physics model, convergence state, or initialisation;
- geometry or material parameters between saved simulations;
- post-processed variable.

A matched-bias calculation should export signed currents for all six terminals, record current balance and use the same initialised device model for both sweep types.

5.3 Resistance-related characteristic

The Combi export reaches about 0.192 at its 30 V endpoint. The original text interpreted this as 192 mΩ. The plot provides neither an expression nor a unit. The apparent secant ratio near 30 V in the output export is about 15 Ω·cm (9–33 Ω·cm across the selected pixels). This range is well above 0.192 Ω·cm, so identifying Combi with V_{DS}/I'_D on the same sweep is unsupported. Converting a reported resistance in Ω would additionally require the device depth and terminal definition.

Use a secant ratio at a specified low drain voltage or the differential slope near the origin. Both require a defined terminal current and gate bias.

$$R_{\text{on,sec}} = V_{\text{DS}}/I_D \tag{5.2}$$

$$R_{\text{on,diff}} = \left(\frac{\partial I_D}{\partial V_{\text{DS}}}\bigg|_{V_{\text{DS}}\to 0^+}\right)^{-1} \tag{5.3}$$

The 0.192 value is a high-end sweep reading of a post-processed quantity. Extracting a resistance requires raw low-voltage current data. A specific resistance also requires A_{active} in equation (1.12).

5.4 Off-state sweep and avalanche comparison

The archived off-state curve reaches about 5 kV without a resolved avalanche rise. The positive endpoint is about 9.6×10^{-10} A/cm after conversion, and earlier excursions reach about -1.9×10^{-8} A/cm. The excursions and small

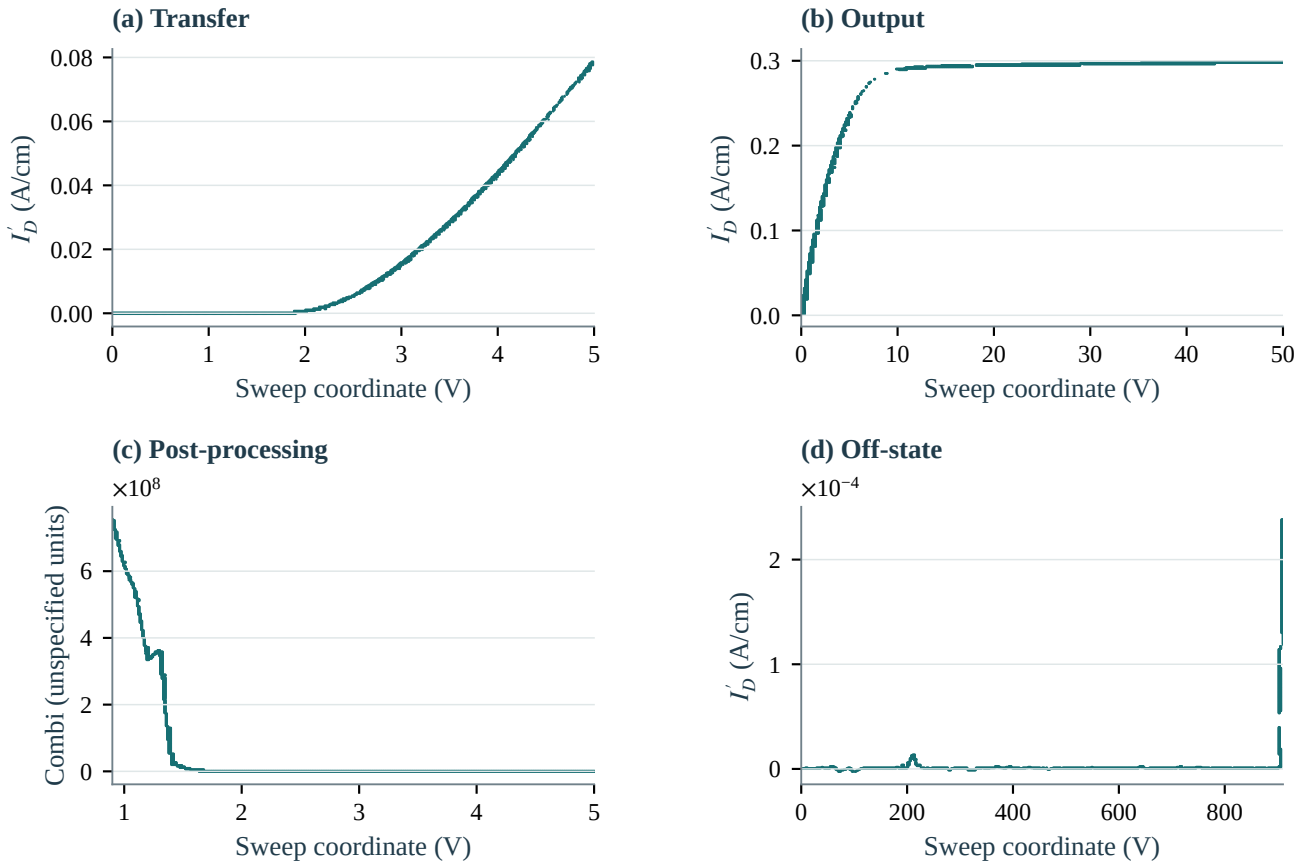

Figure 4.6 – Digitised transfer, output, Combi and off-state sweeps of the vertical SiC structure labelled JFET in the archive. The off-state sweep reaches about 910 V.

positive signal require solver residuals and a documented sign convention for interpretation.

The archived outputs leave four device-level checks unresolved.

1. The impact-ionisation law, coefficients and activation settings are missing from the export.
2. Peak-field maps and mesh-convergence data near the highest biases were not retained with the curve.
3. Thermal boundary conditions and the treatment of temperature-dependent leakage remain unspecified.
4. The signed current, numerical resolution and any post-processing floor need to be checked.

Appendix B predicts 1.96–2.46 kV for a 20 µm uniform layer with an assumed net donor density of $10^{16}\,\mathrm{cm}^{-3}$. A 5 kV sweep without a resolved avalanche rise is therefore inconsistent with the nominal one-dimensional scenario if the current path and ionisation law match. Disabled, incomplete or uncalibrated avalanche physics is one possibility. The Ecorce drift doping, field profile, voltage partition, active models and output criterion are unknown, so the comparison cannot identify the active setting. The 5 kV endpoint is a sweep limit.

5.5 What can be inferred from the complete result set

Observations

The geometry and electrical curves document the simulated topology and the stated sweep ranges. Their digitised readoffs provide estimates at the displayed coordinates.

Device quantities requiring matched bias

A positive threshold, a low-voltage differential resistance and a breakdown rating require explicit current criteria, a common simulation deck and reliable field and terminal-current data.

Repeating both sweep paths through a common bias point would help determine whether the observed difference arises from the simulated state, sweep history or current definition.

5.6 Uncertainty budget

A derived metric m depends on the assumed physical parameters and discretisation.

$$m = f(\theta_{\mathrm{geom}}, \theta_{\mathrm{mat}}, \theta_{\mathrm{contact}}, \theta_{\mathrm{trap}}, \theta_{\mathrm{num}}) \tag{5.4}$$

For small parameter perturbations, a first-order covariance estimate uses the sensitivity row $\mathbf{J}_m$ evaluated at the nominal parameter vector θ.

$$\sigma_m^2 \simeq \mathbf{J}_m \Sigma_\theta \mathbf{J}_m^{\mathrm{T}}, \qquad \mathbf{J}_m = \frac{\partial f}{\partial \theta} \tag{5.5}$$

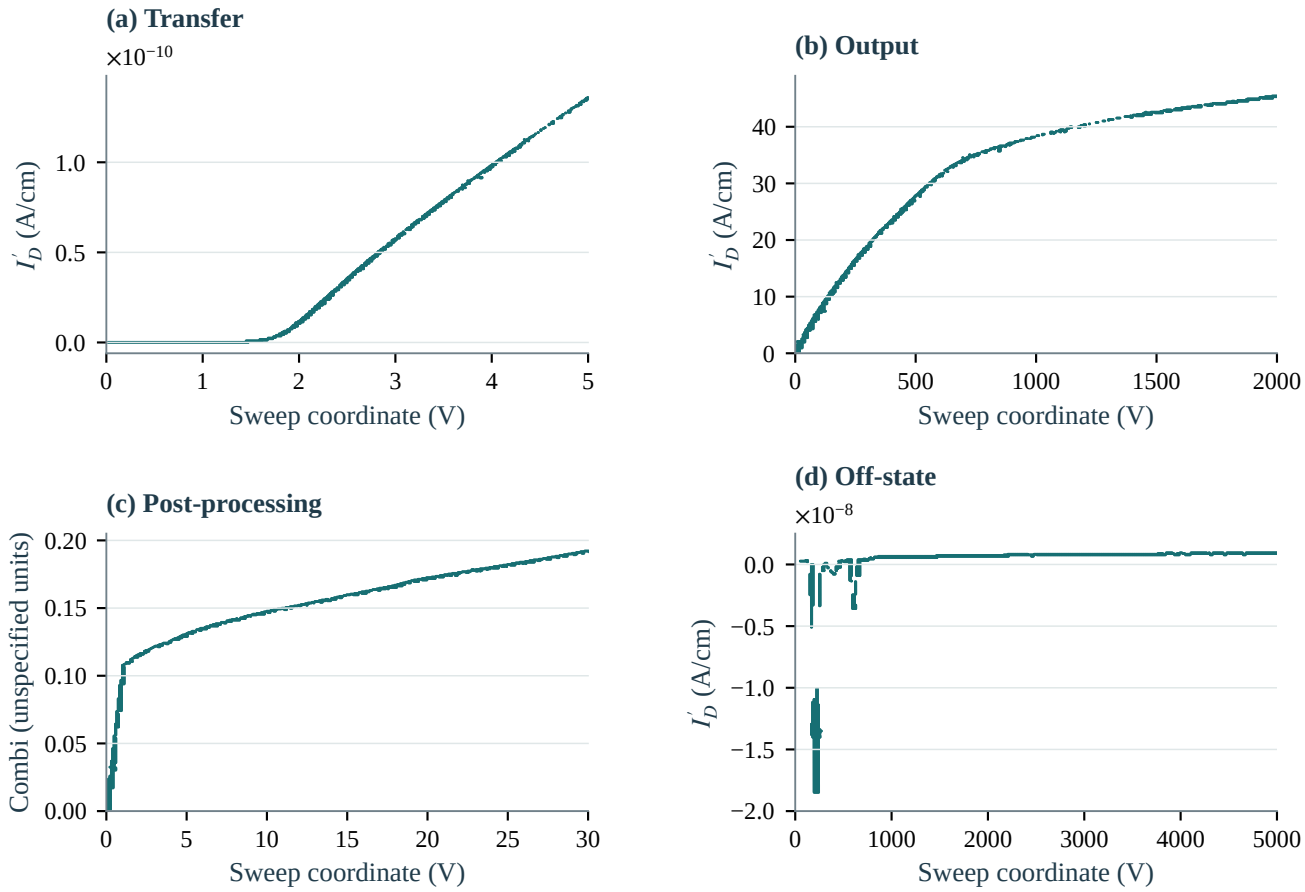

Figure 5.1 – Digitised versions of the four Ecorce sweeps reproduced in Appendix C.5 from [18]. Currents are expressed in A/cm. The three current panels have different ordinate scales. The voltage label preserves the sweep coordinate because the complete terminal-bias vectors are unavailable.

Table 5.1 – Observations and principal limitations of the device exports.

Device	Displayed response	Main limitation	Use in this study
Lateral GaN HEMT	Two transfer traces with different apparent onsets	Complete bias vectors and gate reference unavailable	Heterointerface transport comparison
Lateral SiC MOSFET	Positive apparent turn-on in transfer	Geometry and voltage conditions differ from the other devices	Gate-control comparison
Vertical SiC (labelled JFET)	Opposed source and drain terminals and apparent current modulation	Full-width p^+ region interrupts the n-type path. Series resistance is unresolved.	Vertical layout comparison
VertiGaN	Resistive output trace and very small off-state current	Bias, current expression, drift profile and avalanche settings unavailable	Basis for a matched-bias rerun

Σ_θ represents the input covariance. The approximation requires a differentiable mapping and uncertainty small enough for linearisation.

The dominant sources of variation differ across the metrics.

- V_{TH}: p-GaN activation, interface charge, trap density, work function;
- R_{on}: mobility, contact resistivity, channel width, current normalisation, self-heating;
- V_{BR}: drift doping, edge geometry, impact ionisation, defect-assisted leakage, mesh density;
- thermal capability: substrate conductivity, boundary conditions, heat-spreading geometry.

5.7 Comparison with the benchmark devices

A comparison at equal voltage class and active area requires a common gate-bias convention, a calibrated field model and explicit contact and drift contributions to conduction loss.

6 Validation Programme

6.1 Reproducible TCAD baseline

A version-controlled device model should record geometry, mesh, materials, contacts, interface charge, traps, mobility, impact ionisation, thermal properties and bias scripts. Each simulation should export machine-readable currents and diagnostics.

The following checks give an initial acceptance protocol.

1. verify charge neutrality and equilibrium band alignment at zero bias;
2. verify terminal-current conservation,

$$\varepsilon_I = \frac{|\sum_k I_k|}{\sum_k |I_k|} < \varepsilon_{I,\max} \tag{6.1}$$

3. perform at least three mesh densities and require metric convergence,

$$\delta_m = \frac{|m_{h/2} - m_h|}{|m_{h/2}|} < \varepsilon_m \tag{6.2}$$

4. use the same saved equilibrium state to initialise transfer, output, and off-state sweeps;
5. export branch currents for both mirrored cells and verify equation (3.2);
6. archive the exact expression and units of every post-processed quantity.

6.2 Physics-model hierarchy

The model should be increased in complexity only after each level is validated.

An isothermal drift–diffusion model addresses electrostatics and current continuity. Avalanche and dynamic reliability require the corresponding physical mechanisms, calibration and convergence checks [5, 9, 10, 14, 15].

6.3 Design-of-experiments programme

A structured parameter study should replace manual one-factor tuning. Let the design vector include drift thickness and doping, p-GaN thickness and acceptor concentration, channel spacing, gate length, oxide thickness, interface charge, and contact resistivity. A space-filling design or Latin hypercube can first identify dominant sensitivities, followed by local optimisation and uncertainty propagation.

Recommended primary responses are

$$\begin{aligned}\mathbf{y} = [&V_{TH}, R_{on,sp}, V_{BR}, g_m,\\ &Q_G, E_{max}, \Delta T_{max}, \eta_{sym}]\end{aligned} \tag{6.3}$$

Pareto fronts should be reported rather than a single "best" geometry because lower resistance, higher threshold, and higher breakdown voltage are competing objectives.

6.4 Breakdown and edge termination

The central research risk is electric-field concentration at gate corners, dielectric boundaries, and the transition from channel to drift region. The model should therefore include field plates or termination structures only after the un-terminated field map is understood. Breakdown evaluation must include:

- a calibrated GaN impact-ionisation model;
- local mesh refinement at every field singularity;
- temperature-dependent leakage and self-heating;
- a defined current or ionisation criterion;
- sensitivity to fixed interface charge and geometric rounding.

The reported voltage should be accompanied by the maximum field and its location, not only a terminal current curve.

6.5 Manufacturability and experimental validation

A conceptually plausible cross-section must be mapped to a process flow. The critical process questions are:

1. Can the mirrored vertical channels and central dielectric be formed without high-defect interfaces?
2. Can p-GaN activation and thickness be controlled tightly enough to obtain a stable positive threshold?
3. Can low-resistance source and drain contacts be realised on the required crystal faces?
4. Can the structure be terminated laterally to prevent premature edge breakdown?
5. Can heat be extracted from both cells without creating current imbalance?

A practical experimental sequence would begin with isolated test structures rather than a complete transistor: transmission-line-method contacts, metal–insulator–semiconductor capacitors, p-GaN gated channel coupons, and vertical diode drift stacks. Only after these elements are calibrated should a full six-terminal demonstrator be fabricated.

6.6 Measurement plan

The minimum characterisation matrix should include:

- DC transfer and output curves over temperature, with forward/backward gate sweeps;
- gate and off-state leakage with guarded instrumentation;
- pulsed I–V after drain and gate stress to measure current collapse;
- dynamic R_{on} and recovery time;

Table 6.1 – Proposed hierarchy for a future device-level simulation campaign.

Level	Added physics	Decision enabled
0	Electrostatic equilibrium and analytic junction checks	Geometry, doping and contact checks
1	Isothermal drift–diffusion with low-field mobility	Transfer and low-voltage output consistency
2	High-field mobility, velocity saturation and recombination	Current saturation and output conductance
3	Polarisation and quantum correction or Schrödinger–Poisson	2DEG density and gate control
4	Interface and bulk traps, incomplete ionisation	Threshold stability and dynamic on-resistance
5	Impact ionisation and field-dependent leakage	Breakdown at a stated criterion
6	Electrothermal coupling	Current capability, hot spots and thermal runaway
7	Transient switching with an external circuit	Gate charge, switching loss and converter behaviour

Table 6.2 – Qualitative risk prioritisation for further work. Likelihood labels are engineering judgements.

Risk	Likelihood	Impact	Proposed check
Transfer/output mismatch	High	Critical	Common deck, terminal-current audit and matching bias points
Gate-edge breakdown	High	Critical	Field maps, corner rounding, field plates and termination design
Unstable p-GaN threshold	Medium–high	High	Traps, incomplete ionisation, temperature and hysteresis sweeps
Excess contact resistance	Medium	High	TLM measurements and a process-specific contact model
Central dielectric failure	Medium	Critical	Oxide field, dielectric lifetime and alternative isolation geometries
Current and thermal imbalance	Medium	High	Symmetry metric, electrothermal simulation and independent current sensing
Fabrication complexity	High	High	Process review and staged test structures

- capacitance–voltage and gate-charge measurements;
- breakdown under current compliance, followed by post-stress inspection;
- infrared or thermoreflectance mapping of cell-to-cell temperature imbalance;
- destructive physical analysis to correlate failure sites with simulated peak fields.

Model calibration should be performed against intermediate structures before the final device. This separates uncertainty in materials and interfaces from uncertainty in the architecture itself.

6.7 Contributions and data provenance

Dev Kumar performed the original numerical modelling and prepared this reanalysis. Tanguy Phulpin proposed the device hypothesis and supervised the 2022 work. Alain Michez provided Ecorce guidance. The reanalysis uses the archived geometry and plots, and Appendix B records the independently implemented drift-layer model.

6.8 Risk register

Table 6.2 ranks the main technical risks identified in this reanalysis and the check proposed for each.

6.9 Validation milestones

Progress can be evaluated against five milestones.

1. **Numerical consistency.** Transfer and output traces agree at common bias points. Conservation and mesh checks meet stated tolerances.
2. **Physical calibration.** The contact, trap, avalanche and thermal models have documented inputs and uncertainty.
3. **Fabrication review.** Process and epitaxy specialists review the layer stack, contact sequence and proposed test structures.
4. **Device measurements.** A demonstrator is evaluated for threshold, on-resistance and breakdown using defined criteria.
5. **Converter comparison.** Switching loss and reliability are compared with a reference device at matched voltage and current.

6.10 Reproducibility package

Record the geometry, parameter tables, convergence studies, raw currents, field maps and metric-extraction scripts. Compare bias-matched data with uncertainty estimates. If a full simulation deck cannot be distributed, a reduced example should identify the available inputs and assumptions.

7 Conclusion

The archived data establish the two-cell topology and show a resistive output response. The ratio V_{DS}/I'_D is about 44 Ω·cm at the high-voltage endpoint. The small transfer current and the undefined Combi quantity leave threshold and on-resistance unresolved.

The uniform-layer calculation yields 1.96–2.46 kV at the stated nominal thickness and doping. Testing voltage support in the complete device requires the actual doping profile, the voltage distribution across layers and a calibrated avalanche calculation.

A common Ecorce model with matched bias points, signed terminal currents and field-convergence checks is needed to connect the three electrical sweeps to a single device characteristic.

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[18] D. Kumar, *Conceptual Design and Finite-Element Assessment of a Dual-Channel Vertical Normally-Off GaN Power Transistor*, unpublished internship report on the July 2022 study, GeePs and Université Sorbonne Paris Nord, 41 pp. Reconstructed in 2026 to document and reassess the 2022 simulations. The Ecorce images are reproduced here unchanged from the archived edition.

Table A.1 – Definitions proposed for future extraction from raw numerical data.

Metric	Definition
Threshold voltage	Current-per-depth criterion I'_{crit} with stated drain bias, temperature and sweep direction. Record the gate leakage and depth convention.
Transconductance	$g_m = \partial I_D/\partial V_{\mathrm{GS}}$ after noise-controlled differentiation. State the peak value and bias point.
On-resistance	Low-V_{DS} slope at stated V_{GS} and temperature. Separate channel, drift, access and contact contributions where possible.
Specific on-resistance	$R_{\mathrm{on}}A_{\mathrm{active}}$, with the active-area definition and treatment of contact pads stated.
Breakdown voltage	Drain voltage at a stated I'_{crit}, avalanche criterion or irreversible current rise. State gate bias, temperature and compliance.
Subthreshold slope	$S = (\mathrm{d}\log_{10} I_D/\mathrm{d}V_{\mathrm{GS}})^{-1}$ over a stated current interval.
Dynamic on-resistance	Pulsed ratio of post-stress resistance to static resistance for a stated quiescent drain bias and delay.
Thermal resistance	$R_\theta = \Delta T/P$ with stated boundary conditions and steady or transient regime.

A Metric Extraction and Reproducibility

A.1 Recommended extraction definitions

Table A.1 lists the extraction definitions recommended for future simulations and measurements.

A.2 Simulation record for each figure

Every future curve should be accompanied by:

- repository commit or immutable deck identifier;
- geometry revision and out-of-plane depth;
- material and interface parameter files;
- physical models enabled;
- mesh statistics and refinement rule;
- temperature and thermal boundary conditions;
- terminal mapping and sign convention;
- bias sequence, step size, continuation strategy, and sweep direction;
- nonlinear tolerance, maximum iterations, and residual history;
- terminal-current conservation error;
- raw numerical data and post-processing expression.

A.3 Digitisation of archived curves

The electrical figures were redrawn by mapping coloured trace pixels to the original axes. Digitisation excludes the colour legends and plot labels. It uses a channel spread of at least 18 intensity counts on an 8-bit RGB image. For dark backgrounds the maximum channel value must also be at least 53. The positions of the end ticks define a linear mapping on each axis. Table A.2 records selected calibration points. Upper and lower values within a voltage window reflect pixel selection and line thickness.

In the lateral GaN export A and the VertiGaN output export, the colour-legend endpoints of 3.20×10^{-4} and 4.54×10^{-3} are a factor of 10^4 below the corresponding plotted values in A/cm. This is consistent with values per micrometre before conversion. For VertiGaN Combi the legend extends to 0.265 and the plotted trace to 0.192. The legend alone does not specify the expression or unit.

The lateral GaN Combi reconstruction excludes the vertical raster feature in the first ten pixel columns of the plot, below 0.14 V on the sweep axis.

A one-pixel step in the output abscissa corresponds to 2.86 V. At 30 ± 2.86 V the median selected ordinate is about 2.04 A/cm, with a trace-pixel range of about 0.91–3.31 A/cm. This is a resolution interval, with no statistical interpretation. A reliable low-bias derivative requires the raw solution points.

Historical note. The 2022 text gives 45.6 A/cm at the output endpoint. This revision uses the axis read-off of approximately 45.4 A/cm.

A.4 Suggested experimental test structures

A first fabrication lot should prioritise parameter identification over full-device performance. Suggested structures are:

1. TLM patterns for each source/drain metallisation stack;
2. p-GaN sheet-resistance and Hall structures;
3. MOS capacitors for Q_f, D_{it}, leakage, and dielectric breakdown;
4. gated Hall bars for channel density and mobility versus gate bias;
5. vertical GaN diodes with multiple drift thicknesses and terminations;
6. single-cell vertical transistors before the mirrored six-terminal device;
7. mirrored cells with separate current sensing to measure η_{sym}.

B Independent electrostatic and avalanche calculation

This appendix reports calculations added in the 2026 reanalysis. The one-dimensional model uses dimensions suggested by the 2022 geometry, published ionisation coefficients and explicit assumptions for missing material inputs. It is an independent calculation for a uniform slab.

B.1 Orientation and charge assumptions

At an abrupt AlGaN/GaN interface, let the unit normal point from GaN to AlGaN. The bound sheet charge follows from the divergence of the spontaneous and piezoelectric polarisa-

Table A.2 – Pixel coordinates refer to the archived raster images. Native ordinate values are listed before conversion.

Trace	x pixels	Bias (V)	y pixels	Native ordinate	Unit
GaN transfer A	140 to 840	0 to 15	811 to 110	0 to 3.2	A/cm
GaN transfer B	140 to 840	−5 to 10	811 to 110	0 to 19.5	A/cm
VertiGaN transfer	219 to 919	0 to 5	839 to 138	0 to 1.36×10^{-14}	A/µm
VertiGaN output	157 to 857	0 to 2000	817 to 117	0 to 45.4	A/cm
VertiGaN Combi	167 to 867	0 to 30	829 to 129	0 to 0.192	unspecified
VertiGaN off-state	251 to 951	0 to 5000	819 to 118	-1.86×10^{-12} to 9.56×10^{-14}	A/µm

tion [2].

$$\sigma_b = (\mathbf{P}_{GaN} - \mathbf{P}_{AlGaN}) \cdot \hat{\mathbf{n}} \tag{B1}$$

For a common crystal orientation and identical polarisation contrast, reversing the normal reverses the charge sign. If the polarisation lies along the wafer-normal c axis, an ideal vertical nonpolar sidewall has zero normal projection. Geometric mirroring alone therefore cannot establish two equivalent electron-accumulation sheets. Crystal polarity, strain, interface charge and the carrier supply need to be stated for each cell.

The polarisation contrast $\Delta P = 0.015\,\mathrm{C/m^2}$ is an assumed sensitivity value, informed by the order of magnitude of AlGaN/GaN polarisation discontinuities [2]. It is not extracted from the archived cross-section. Full normal projection gives 9.36×10^{12} elementary charges per $\mathrm{cm^2}$. With an assumed ionised acceptor density of $10^{18}\,\mathrm{cm^{-3}}$, a fully depleted 50 nm p-GaN layer supplies $5.0 \times 10^{12}\,\mathrm{cm^{-2}}$. Approximately 94 nm would balance the assumed magnitude. Threshold prediction also requires band offsets, gate potential, carrier supply and traps.

B.2 Uniform drift-layer model

The longitudinal calculation represents a one-sided p^+/n^- GaN junction. The uniform layer is assumed to be 20 µm thick for the nominal scenario, with net donor density $N_D = 10^{16}\,\mathrm{cm^{-3}}$. The thickness is taken from the nominal device height. The assumed doping is a parameter of the sensitivity study, because the original drift doping is unavailable. The field is parallel to the c axis, $\varepsilon_r = 10.6$ is taken from [16], donors are treated as ionised and the built-in voltage is neglected relative to kilovolt bias. The field slope is $k = qN_D/\varepsilon$.

$$V_{FD} = \frac{kL^2}{2}, \qquad w = \min\left(L, \sqrt{2V/k}\right)$$
$$E(z) = V/w + k(w/2 - z), \qquad 0 \le z \le w \tag{B2}$$

The peak field is at $z = 0$. Before full depletion it vanishes at w. After full depletion the field at the rear contact increases with voltage. Lateral crowding, gate leakage, traps, tunnelling and thermal feedback require a device-level model.

B.3 Impact-ionisation model

Let α and β be the electron and hole impact-ionisation coefficients. For carriers moving in opposite directions, the homogeneous injection condition gives the following criterion for self-sustaining multiplication.

$$F_{av}(V) = \int_0^w \alpha(z) \exp\left[\int_0^z (\beta - \alpha)\,\mathrm{d}s\right] \mathrm{d}z = 1 \tag{B3}$$

The first root defines V_A. The two published coefficient sets in Table B.1 use $\alpha = a_n \exp(-b_n/E)$ and $\beta = a_p \exp(-b_p/E)$ [14, 15].

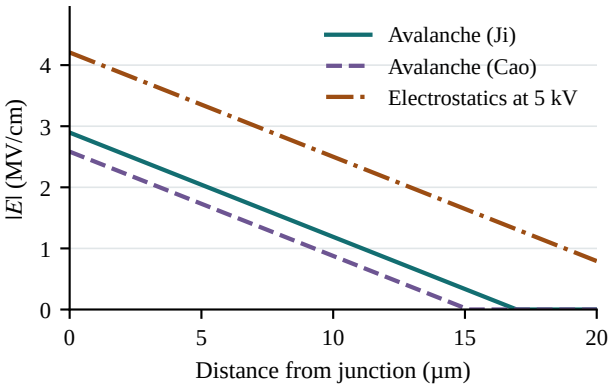


Figure B.1 – Longitudinal field in the nominal drift layer. The 5 kV profile is an electrostatic continuation beyond the two calculated avalanche roots.

B.4 Results and model sensitivity

At the assumed nominal values $L = 20\,\mu\mathrm{m}$ and $N_D = 10^{16}\,\mathrm{cm^{-3}}$, full depletion occurs at 3.41 kV. The electrostatic continuation to 5 kV gives a mean field of 2.50 MV/cm and a peak of 4.21 MV/cm. The Ji and Cao models reach avalanche at 2.46 and 1.96 kV, with corresponding peak fields of 2.90 and 2.58 MV/cm and depleted widths of 16.96 and 15.14 µm. Figure B.1 compares these profiles.

For a uniform layer of thickness L, donor density N_D and electron mobility μ_n, the drift resistance normalised to the conducting GaN area is

$$R_{d,sp} = \frac{L}{q\mu_n N_D} \tag{B4}$$

At an assumed $N_D = 3 \times 10^{15}\,\mathrm{cm^{-3}}$, the 5 kV thicknesses are about 25.8 µm with Ji and 39.8 µm with Cao. For an assumed $\mu_n = 900\,\mathrm{cm^2/(V\,s)}$, these thicknesses give about 5.96 and 9.20 $\mathrm{m\Omega{\cdot}cm^2}$, respectively.

Table B.1 – Published coefficients used in the independent calculation. These are two alternative models.

Fit	a_n (cm^{-1})	b_n (V/cm)	a_p (cm^{-1})	b_p (V/cm)
Ji [14]	2.11×10^9	3.689×10^7	4.39×10^6	1.80×10^7
Cao [15]	4.48×10^8	3.39×10^7	7.13×10^6	1.46×10^7

Table B.2 – Calculated avalanche roots and drift resistance for the stated uniform-layer model. Mobility is an assumed scenario input.

L (µm)	N_D (cm^{-3})	Ji (kV)	Cao (kV)	$R_{\mathrm{d,sp}}$ (mΩ·cm^2)
10	10^{16}	2.04	1.73	0.69
20	3×10^{15}	4.18	3.53	4.62
20	10^{16}	2.46	1.96	1.39
20	2×10^{16}	1.40	1.14	0.69
30	3×10^{15}	5.50	4.52	6.94
40	3×10^{15}	6.30	5.01	9.25

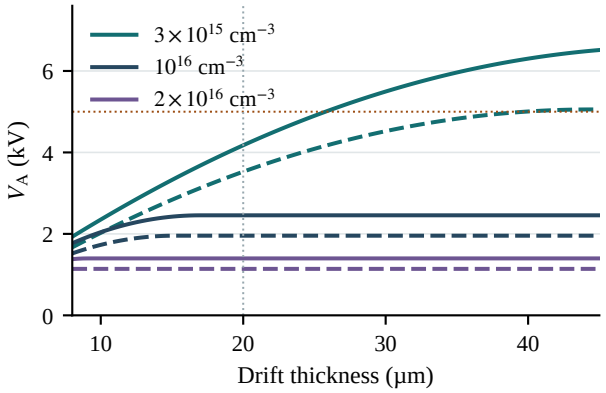


Figure B.2 – Avalanche voltage versus drift thickness. Solid and dashed curves use the Ji and Cao laws. Each colour is one donor density.

In Figure 3.2 the fraction of the footprint occupied by GaN is $(2 \times 3\,\mu\mathrm{m})/(10\,\mu\mathrm{m}) = 0.60$. For current confined to these strips, the footprint-normalised specific drift resistance is $1/0.60 \approx 1.67$ times the value normalised to the conducting GaN area.

Table B.2 summarises the avalanche roots and drift resistances. Reducing ε_r from 10.6 to 9.5 lowers the nominal roots by 8.5% and 8.2% for Ji and Cao. Suppressing both rates below 2 MV/cm raises them by 0.05% and 0.68%. The models give distinct high-field predictions and do not define a statistical confidence interval. A full transistor can fail through field crowding or dielectric leakage before the uniform slab reaches avalanche.

B.5 Numerical checks and implementation

The calculation uses 4,096 cells and midpoint fields. Within each cell the rates are held constant and the exponential contribution is integrated analytically. The code below evaluates the integral and finds its first root. L is in micrometres and `Nd` in cm^{-3}. The result is in volts. For the nominal scenario use `avalanche(20, 1e16, JI)`, with `CAO` for the second law.

Across 24 combinations of four layer thicknesses, three donor densities and two laws, changing the grid from 4,096 to 1,024 cells changes the root by at most 6.2×10^{-4} V. Using 8,192 cells changes it by at most 3.1×10^{-5} V. An independent adaptive Runge–Kutta integration reproduces the roots within 4.1×10^{-5} V. These checks quantify numerical convergence for this reduced model.

```
import numpy as np
from scipy.optimize import brentq

Q = 1.602176634e-19        # C
EPS0 = 8.8541878128e-14    # F/cm
JI = (2.11e9, 3.689e7, 4.39e6, 1.80e7)
CAO = (4.48e8, 3.39e7, 7.13e6, 1.46e7)

def avalanche(L, Nd, law, cells=4096, er=10.6,
              emin=0.0):
    length = L * 1e-4
    k = Q * Nd / (EPS0 * er)
    an, bn, ap, bp = law

    def residual(v):
        if v == 0.0:
            return -1.0
        w = min(length, np.sqrt(2 * v / k))
        dz = w / cells
        z = (np.arange(cells) + .5) * dz
        e = v / w + k * (w / 2 - z)
        e = np.maximum(e, 1e-30)
        a = an * np.exp(-bn / e) * (e >= emin)
        b = ap * np.exp(-bp / e) * (e >= emin)
        d = (b - a) * dz
        s = np.r_[0, np.cumsum(d[:-1])]
        f = np.ones_like(d)
        np.divide(np.expm1(d), d, out=f,
                  where=d != 0)
        return np.sum(a * dz * np.exp(s) * f) - 1

    w = min(length, 4e6 / k)
    upper = w * (4e6 - .5 * k * w)
    return brentq(residual, 0, upper, xtol=1e-8)
```

The original six-terminal device requires its own carrier transport and field calculation. A future run should record the bias vector, signed terminal currents, charge balance, physical models, residuals and peak-field convergence. The slab thresholds provide a reference for the assumed bulk material, as discussed in section 5.4.

C Original Ecorce benchmark exports and model views

The 2022 internship report [18] is the source of the Ecorce images. The panels retain the original axes, colour legends and French labels. Page references in the captions refer to the archived PDF.

C.1 Silicon diode and lateral GaN HEMT

(a) Silicon diode **(b) Lateral GaN transfer A**

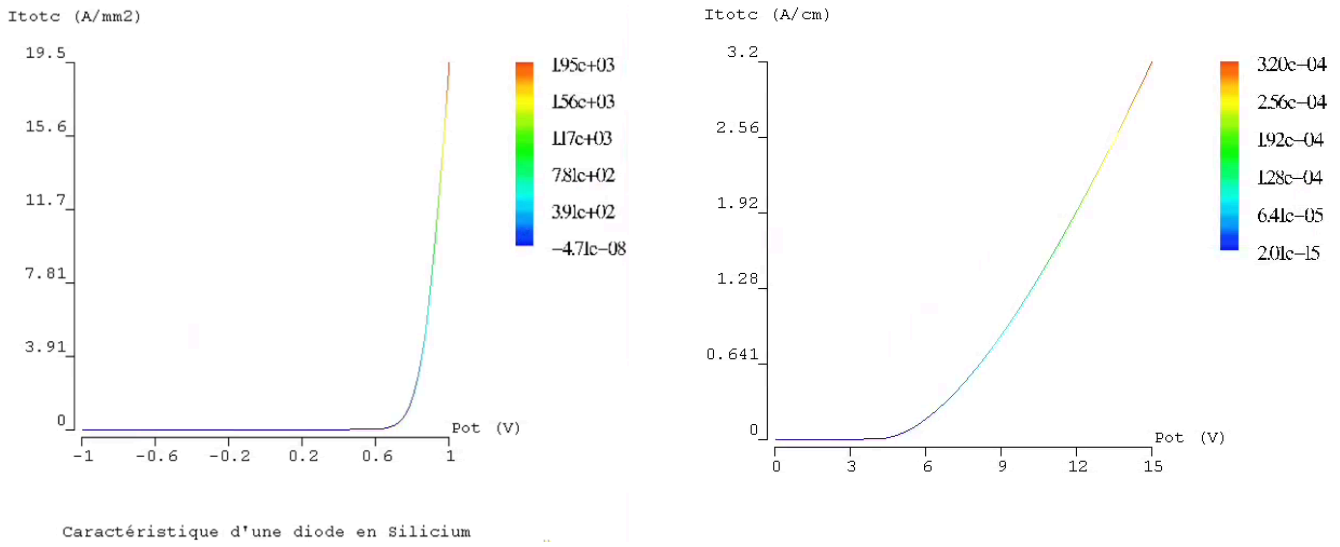


Figure C.1 – Original Ecorce silicon-diode plot (a) and lateral GaN transfer A (b) from [18], PDF pp. 15 and 26. The digitised traces are in Figures 1.1 and 4.1b.

(a) Lateral GaN transfer B **(b) Lateral GaN Combi**

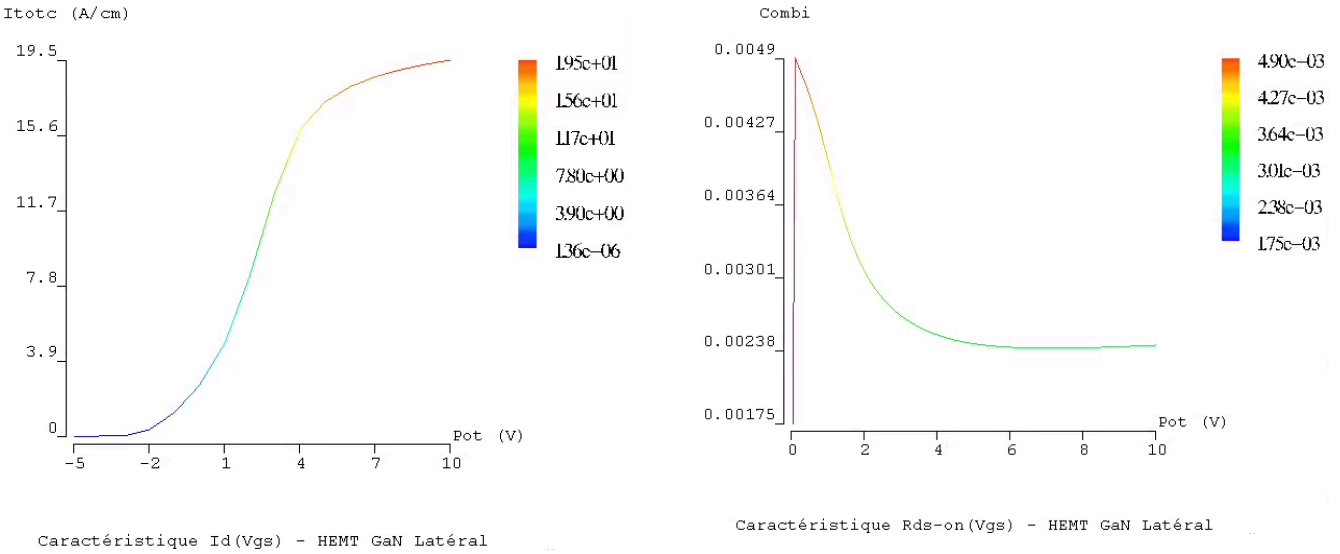
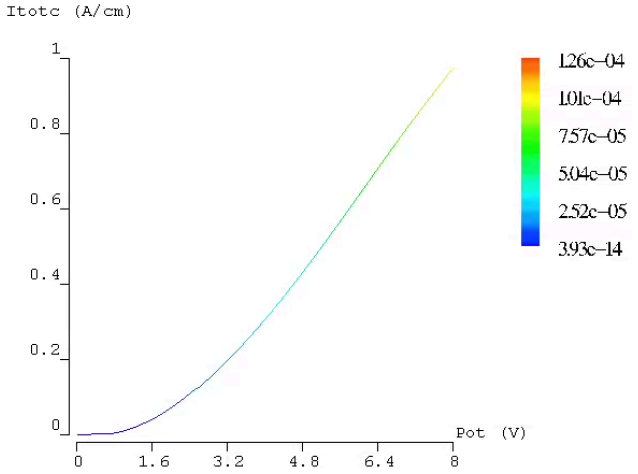


Figure C.2 – Original lateral GaN transfer B (a) and Combi (b) from [18], PDF p. 27. Figure 4.2 gives the digitised traces. Appendix A.3 describes the feature near the origin.

C.2 Lateral SiC MOSFET

(a) Lateral SiC MOSFET transfer



(b) Lateral SiC MOSFET output

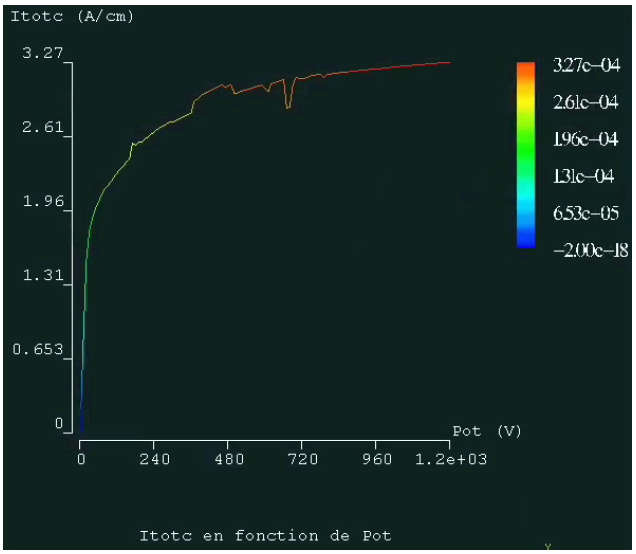
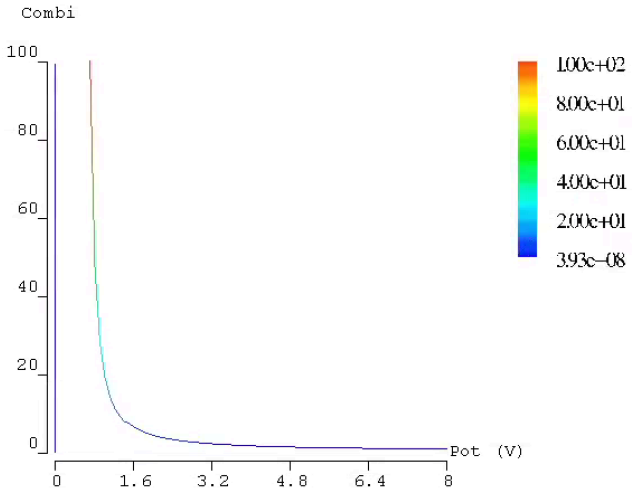


Figure C.3 – Original Ecorce lateral SiC MOSFET transfer (a) and output (b) from [18], PDF p. 27. The digitised traces are in Figures 4.3b and 4.4a.

(a) Lateral SiC MOSFET Combi



(b) Lateral SiC MOSFET off-state

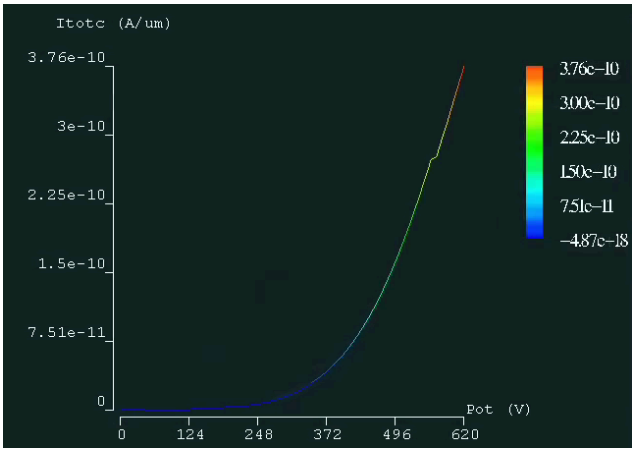


Figure C.4 – Original Ecorce lateral SiC MOSFET Combi (a) and off-state sweep (b) from [18], PDF p. 27. The digitised traces are in Figures 4.4b and 4.4c.

C.3 Vertical SiC structure (labelled JFET)

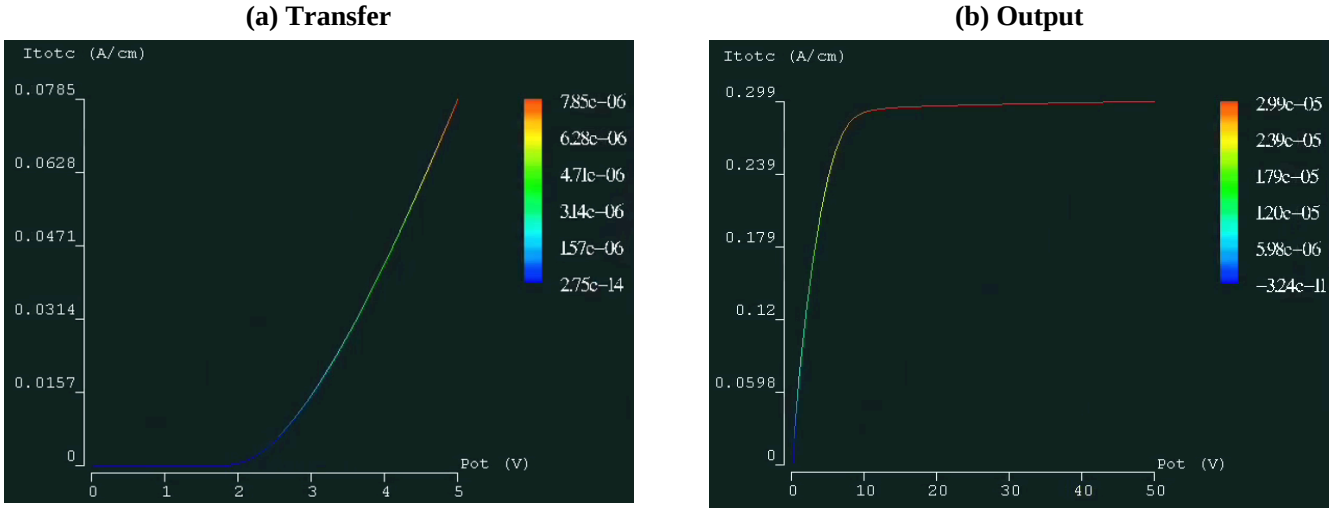


Figure C.5 – Transfer (a) and output (b) of the SiC structure labelled JFET, [18], PDF p. 29. See Figure 4.6.

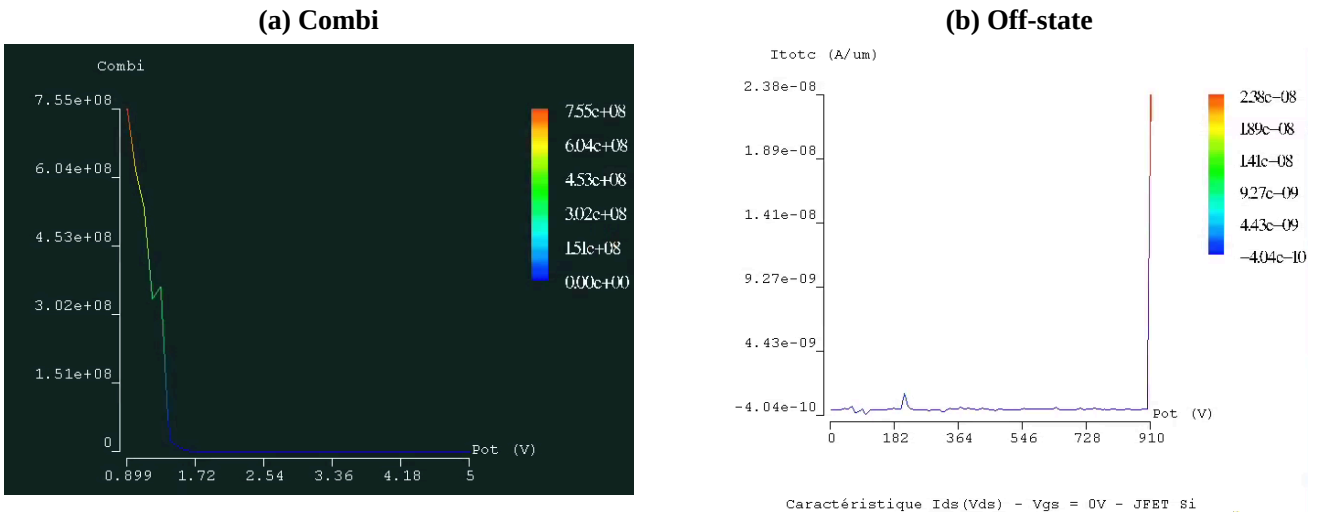


Figure C.6 – Original Combi (a) and off-state sweep (b) of the vertical SiC structure labelled JFET in [18], PDF p. 29. The label JFET Si is visible in panel (b). Figure 4.6 gives the digitised traces.

C.4 Geometries and internal quantities

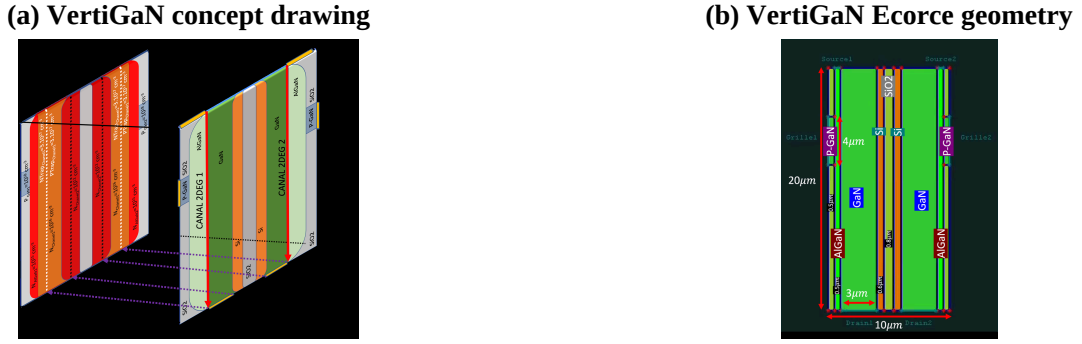


Figure C.7 – VertiGaN concept (a) and cross-section (b) from [18], PDF pp. 21–22. See Figures 3.1–3.2.

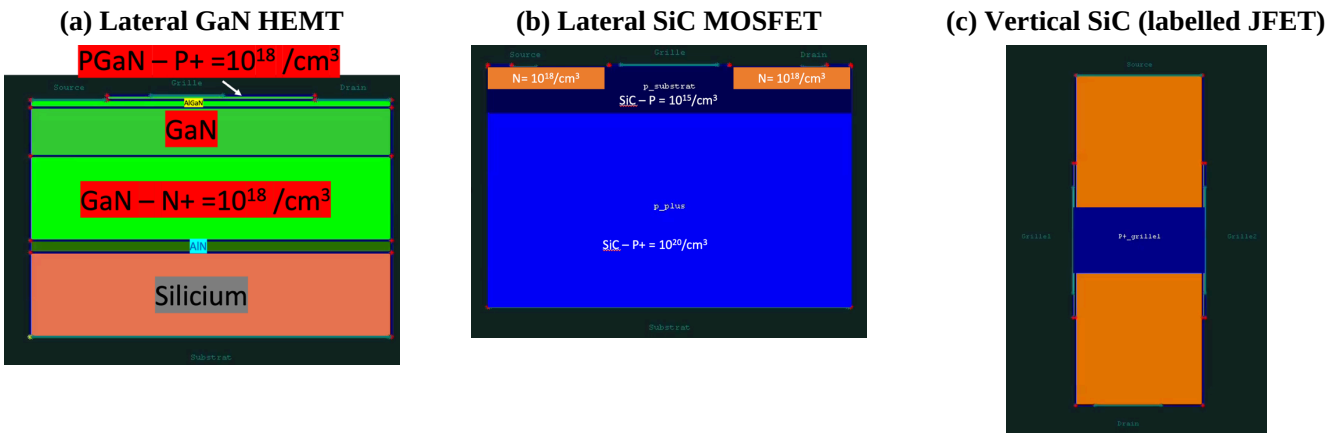


Figure C.8 – Ecorce cross-sections of the lateral GaN HEMT (a), lateral SiC MOSFET (b) and SiC structure labelled JFET (c) from [18], PDF pp. 26–28.

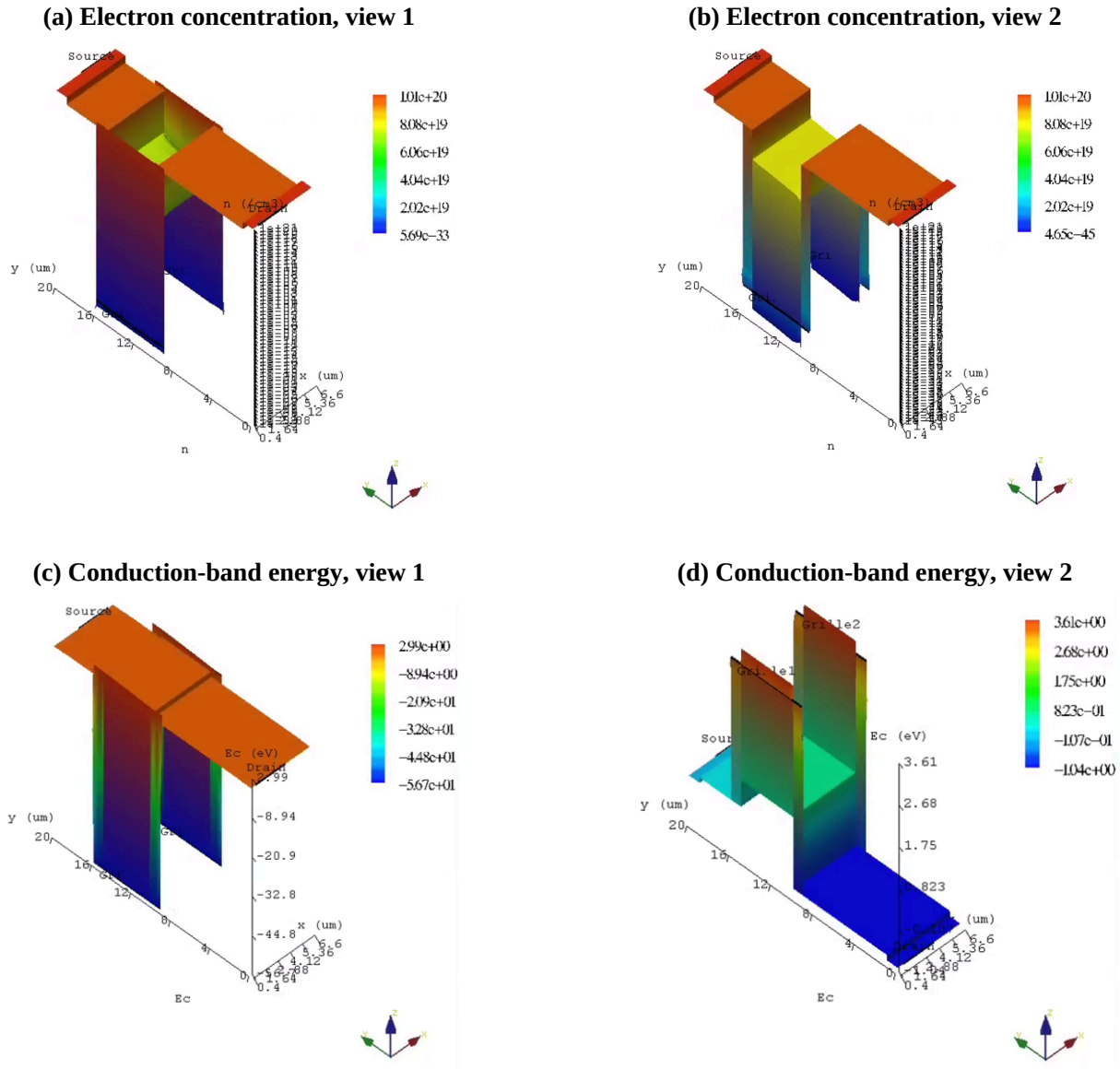


Figure C.9 – Electron concentration (a–b) and conduction-band energy (c–d) for the SiC structure labelled JFET in [18], PDF p. 28. Quantitative comparison requires the original bias conditions and raw field data.

C.5 Original VertiGaN electrical exports

(a) VertiGaN transfer **(b) VertiGaN output**

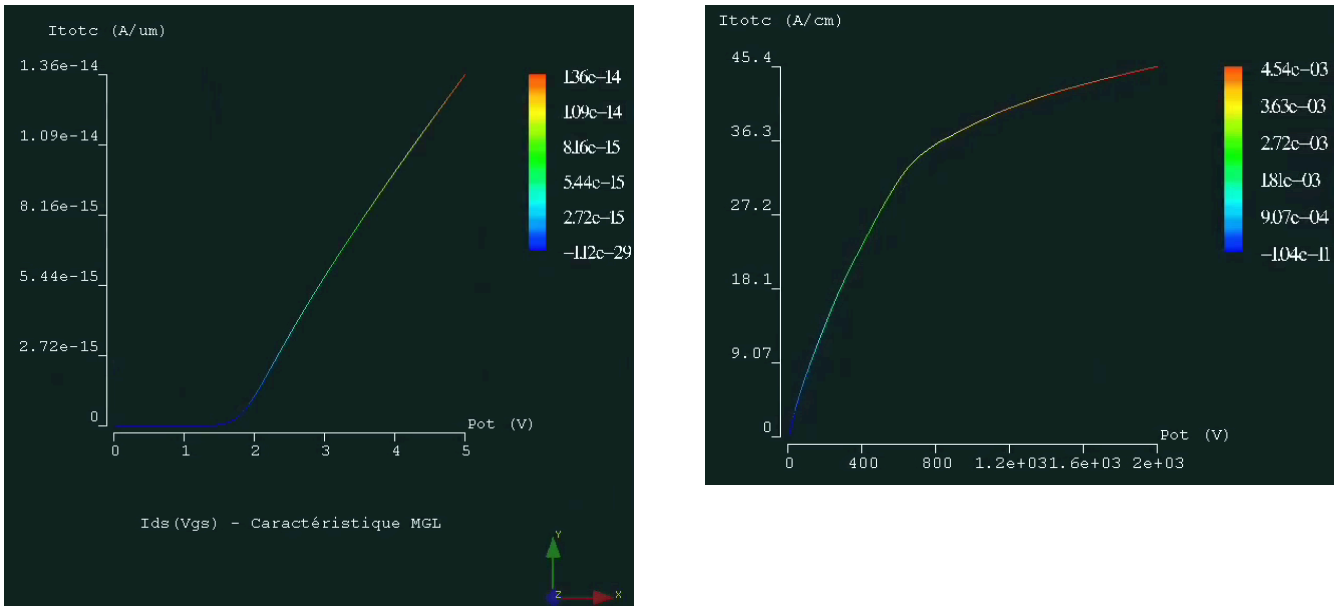


Figure C.10 – Original Ecorce VertiGaN transfer (a) and output (b) from [18], PDF p. 30. The axes and colour legends follow the archive.

(a) VertiGaN Combi **(b) VertiGaN off-state**

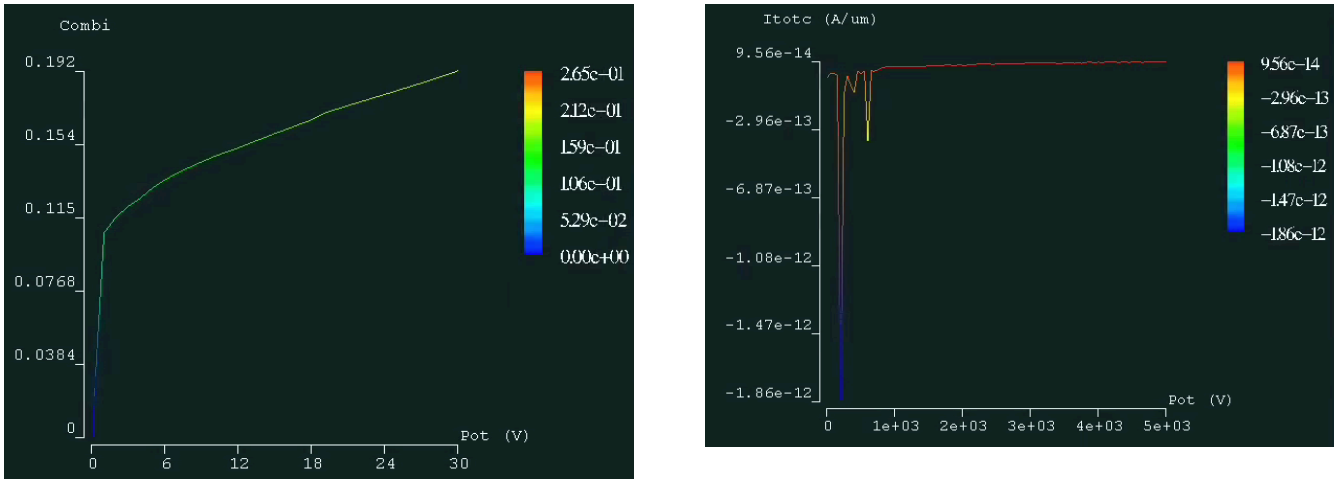


Figure C.11 – Original Ecorce VertiGaN Combi (a) and off-state (b) from [18], PDF p. 30. Figure 5.1 gives the digitised curves. Appendix A.3 discusses the displayed scales.